High Speed ADC FIFO Evaluation Kit

HSC-ADC-EVAL-SC/HSC-ADC-EVAL-DC

FEATURES

Buffer memory board for capturing digital data
Used with high speed ADC evaluation boards
Two 32K FIFOs
Simplifies evaluation of high speed ADCs
Measures performance with ADC Analyzer™ software
- **Real-time FFT and time-domain analysis**
- **Analyze SNR, SINAD, SFDR, and harmonics**
- **Import raw text data for analysis**

Simple PC parallel port interface
Compatible with Windows® 95, Windows 98, Windows 2000, and Windows NT®

EQUIPMENT NEEDED

3.3 V power supply
Parallel printer cable (IEEE-1284 compatible)
Analog signal source and antialiasing filter
Low jitter clock source
High speed ADC evaluation board and ADC data sheet
PC running Windows 95, Windows 98, Windows 2000, or Windows NT

PRODUCT DESCRIPTION

The high speed ADC FIFO evaluation kit includes a memory board to capture blocks of digital data from Analog Devices' high speed analog-to-digital converter (ADC) evaluation boards and ADC Analyzer software. This FIFO board can be connected to a PC through a standard printer cable and used with the ADC Analyzer software to quickly evaluate the performance of high speed ADCs. Users can view an FFT for a specific analog input and clock rate and analyze SNR, SINAD, SFDR, and harmonic information.

The evaluation kit is easy to set up. Additional equipment needed includes an Analog Devices' high speed ADC evaluation board, a power supply, a signal source, and a clock source. Once the kit is connected and powered, the evaluation is instantly enabled on the PC.

Two versions of the FIFO are available. The HSC-ADC-EVAL-DC is used with dual ADCs and converters with demultiplexed digital outputs. The HSC-ADC-EVAL-SC evaluation board is used with single-channel ADCs. Users should see Table 1 to choose the FIFO appropriate for their high speed ADC evaluation board.

FUNCTIONAL BLOCK DIAGRAM

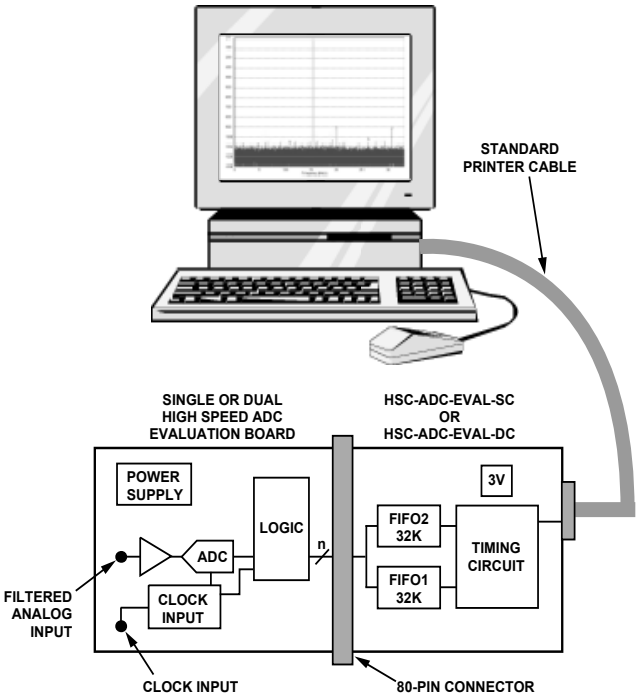

Figure 1. Functional Block Diagram (Simplified)

PRODUCT HIGHLIGHTS

1. **Two 32K FIFOs—**These FIFOs store data from the ADC(s) for processing. Pin compatible FIFO family used for easy upgrade.
2. **Up to 133 MSPS clock rate on each channel—**Single-channel ADCs with clock rates up to 133 MSPS can be used with the FIFO board. Dual ADCs and converters with demultiplexed digital outputs can also be used with the FIFO board (with clock rates up to 133 MSPS on each output channel).
3. **Adjustable timing for dual-channel ADCs—**Easily adjust timing to ensure data is captured correctly.
4. **Easy to set up—**Connect the two evaluation boards, power supplies, and signal sources to the PC and instantly evaluate the performance.

Rev. A

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REVISION HISTORY

Revision A

4/03—Data Sheet Changed from REV. 0 to REV. A

Added Figure 2 4
Edit to Figure 33 30

QUICK START

REQUIREMENTS INCLUDE THE FOLLOWING:

- FIFO evaluation board and ADC Analyzer software
- High speed ADC evaluation board and ADC data sheet
- 3.3 V power supply for FIFO evaluation board
- Power supply for ADC evaluation board
- Analog signal source and appropriate filtering
- Low jitter clock source applicable for specific ADC evaluation, typically < 1 ps rms
- Parallel printer cable (IEEE-1284 compatible)
- PC running Windows 95, Windows 98, Windows 2000, or Windows NT

QUICK START STEPS

1. Connect the FIFO evaluation board to the ADC evaluation board. If an adapter is required, insert the adapter between the ADC evaluation board and the FIFO board. If using the HSC-ADC-EVAL-SC model, connect the evaluation board to the bottom half of the 80-pin connector (closest to the installed IDT FIFO chip).

2. Connect a parallel printer cable to the FIFO evaluation board and to LPT1 or LPT2 on the computer.

   Note that the FIFO board is controlled through a PC's parallel (printer) port. For valid data transfer and control, the PC parallel port must be IEEE-1284 compatible in Bidirectional Mode (standard bidirectional). This should not be an issue with newer PCs. Users who do not know how their PCs are configured should consult their manual for information on running the BIOS setup program. It is recommended that users with more than one port disconnect any printers connected to their PCs before running the software for the first time, or if users change the port where the board is connected.

3. Refer to Table 4 for any jumper changes. Most evaluation boards can be used with the default settings.

4. Connect the appropriate power supplies to the FIFO and ADC evaluation boards. The FIFO evaluation board requires a 3.3 V power supply. Refer to the instructions included with the ADC data sheet for more information about the ADC evaluation board setup.

5. Apply power to both evaluation boards and check the voltage levels at the board level.

6. Connect the appropriate analog input (which should be filtered with a band-pass filter) and low jitter clock signal. Make sure the evaluation boards are powered before connecting the analog input and clock.

7. Start the ADC Analyzer software (see the Installation section for installing the software).

8. Choose a configuration file for the ADC evaluation board used or create one (see the Configuring an Evaluation Board section for more information).

9. Click on the time data button (left-most button under the pull-down menus). A reconstruction of the analog input will appear. If the expected signal does not appear, or if there is only a flat red line, refer to the Troubleshooting section for more information.

Definitions

Harmonic Distortion, Second

The ratio of the rms signal amplitude to the rms value of the second harmonic component, reported in dBc.

Harmonic Distortion, Third

The ratio of the rms signal amplitude to the rms value of the third harmonic component, reported in dBc.

Signal-to-Noise-and-Distortion (SINAD)

The ratio of the rms signal amplitude (set 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics but excluding dc.

Signal-to-Noise Ratio (Without Harmonics)

The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

Spurious-Free Dynamic Range (SFDR)

The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. It also may be reported in dBc (i.e., degrades as signal level is lowered) or dBFS (i.e., always related back to converter full scale).

Two-Tone SFDR

The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. It also may be reported in dBc (i.e., degrades as signal level is lowered) or in dBFS (i.e., always relates back to converter full scale).

Worst Other Spur

The ratio of the rms signal amplitude to the rms value of the worst spurious component (excluding the second and third harmonics) reported in dBc.

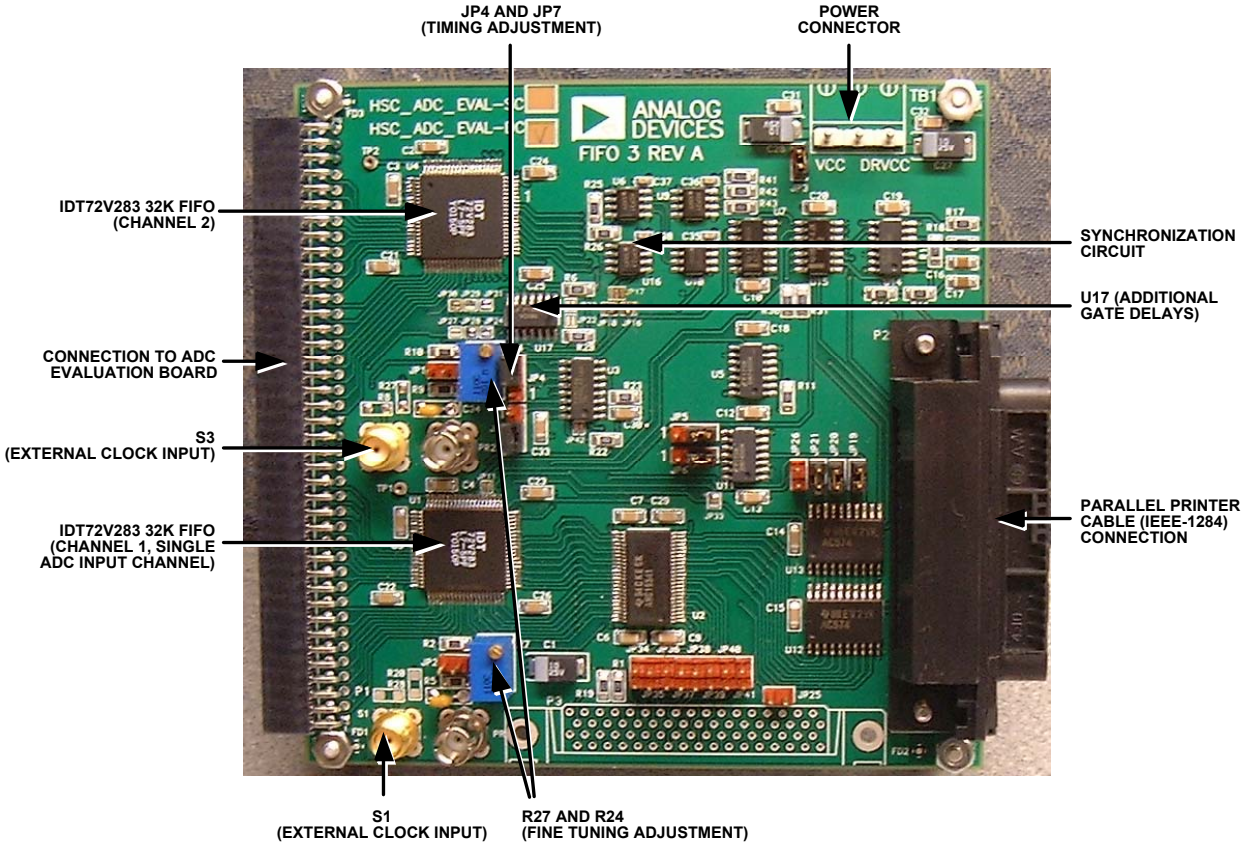


Figure 2. FIFO Components

OPERATION

Supported Evaluation Boards

The following evaluation boards can be used with the high speed ADC FIFO Evaluation Kit[1]. Some evaluation boards require an adapter between the ADC evaluation board connector and the FIFO connector. Some adapters are included; however, if an adapter is needed, send an email to highspeed.converters@analog.com with the part number of the adapter and a mailing address.

HSC-ADC-EVAL-DC AND HSC-ADC-EVAL-SC COMPATIBLE EVALUATION BOARDS[2]

Evaluation Board Model	Description of ADC	Comments
HSC-ADC-EVAL-DC		
AD9059/PCB	Dual 8-Bit, 60 MSPS ADC	Requires AD9059FFA
AD9289BBC-65EB	Quad 8-Bit, 65 MSPS ADC[3]	
AD9480BSU-250EB	8-Bit, 250 MSPS ADC	
AD9410/PCB	10-Bit, 210 MSPS ADC	
AD9430-CMOS/PCB	12-Bit, 210 MSPS ADC	
AD9218-105PCB	Dual 10-Bit, 105 MSPS ADC	
AD9218-65PCB	Dual 10-Bit, 65 MSPS ADC	
AD9238-20PCB	Dual 12-Bit, 20 MSPS ADC	
AD9238-40PCB	Dual 12-Bit, 40 MSPS ADC	
AD9238-65PCB	Dual 12-Bit, 65 MSPS ADC	
AD10265/PCB	Dual 12-Bit, 65 MSPS ADC	Requires LG-0204A
AD13280/PCB	Dual 12-Bit, 80 MSPS ADC	Requires LG-0204A
AD10200/PCB	Dual 12-Bit, 105 MSPS ADC	Requires LG-0204A
AD10201/PCB	Dual 12-Bit, 105 MSPS ADC	Requires LG-0204A
AD10226/PCB	Dual 12-Bit, 125 MSPS ADC	Requires LG-0204A
AD10235/PCB	Dual 12-Bit, 215 MSPS ADC	Requires LG-0204A
AD10465/PCB	Dual 14-Bit, 65 MSPS ADC	Requires LG-0204A
AD13465/PCB	Dual 14-Bit, 65 MSPS ADC	Requires LG-0204A
AD10401/PCB	Dual 14-Bit, 105 MSPS ADC	Requires LG-0204A
HSC-ADC-EVAL-SC		
AD9281-EB	Dual 8-Bit, 28 MSPS ADC[4]	Requires AD922xFFA
AD9280-EB	8-Bit, 32 MSPS ADC	Requires AD922xFFA
AD9057/PCB	8-Bit, 80 MSPS ADC	Requires AD9283FFA
AD9283/PCB	8-Bit, 100 MSPS ADC	Requires AD9283FFA
AD9200SSOP-EVAL	10-Bit, 20 MSPS ADC	Requires AD922xFFA
AD9200TQFP-EVAL	10-Bit, 20 MSPS ADC	Requires AD922xFFA
AD9201-EVAL	Dual 10-Bit, 20 MSPS ADC[4]	Requires AD922xFFA
AD9203-EB	10-Bit, 40 MSPS ADC	Requires AD922xFFA
AD9051/PCB	10-Bit, 60 MSPS ADC	Requires AD9051FFA
AD9214-65PCB	10-Bit, 65 MSPS ADC	
AD9215BRU-65EB	10-Bit, 65 MSPS ADC	
AD9215BCP-65EB	10-Bit, 65 MSPS ADC	
AD9215BRU-80EB	10-Bit, 80 MSPS ADC	
AD9215BCP-80EB	10-Bit, 80 MSPS ADC	
AD9071/PCB	10-Bit, 100 MSPS ADC	Requires AD9071FFA
AD9214-105PCB	10-Bit, 105 MSPS ADC	
AD9215BRU-105EB	10-Bit, 105 MSPS ADC	
AD9215BCP-105EB	10-Bit, 105 MSPS ADC	

[1] Send an email to highspeed.converters@analog.com for information on evaluating the AD9288 with the High Speed ADC FIFO Evaluation Kit.
[2] Connector pin numbers and/or labeling on some evaluation boards (AD9214, AD9410, AD9430, AD9433, AD9235, and AD9244) may not match the FIFO connector numbering; however, the physical connections are correct.
[3] The High Speed ADC FIFO Evaluation kit can be used to evaluate two channels of the AD9289 at a time.
[4] The AD9281 and AD9201 have a single output bus.

HSC-ADC-EVAL-DC AND HSC-ADC-EVAL-SC COMPATIBLE EVALUATION BOARDS[1] (CONTINUED)

Evaluation Board Model	Description of ADC	Comments
HSC-ADC-EVAL-SC (continued)		
AD9221-EB	12-Bit, 1.25 MSPS ADC	Requires AD922xFFA
AD9223-EB	12-Bit, 3 MSPS ADC	Requires AD922xFFA
AD9220-EB	12-Bit, 10 MSPS ADC	Requires AD922xFFA
AD9235-20PCB	12-Bit, 20 MSPS ADC	
AD9235BCP-20EB	12-Bit, 20 MSPS ADC	
AD9225-EB	12-Bit, 25 MSPS ADC	Requires AD922xFFA
AD9224-EB	12-Bit, 40 MSPS ADC	Requires AD922xFFA
AD9235-40PCB	12-Bit, 40 MSPS ADC	
AD9235BCP-40EB	12-Bit, 40 MSPS ADC	
AD9235-65PCB	12-Bit, 65 MSPS ADC	
AD9235BCP-65EB	12-Bit, 65 MSPS ADC	
AD9226-EB	12-Bit, 65 MSPS ADC	Requires AD922xFFA
AD9226QFP-EB	12-Bit, 65 MSPS ADC	Requires AD922xFFA
AD6640ST/PCB	12-Bit, 65 MSPS ADC	Requires AD664xFFA[2]
AD9236BRU-80EB	12-Bit, 80 MSPS ADC	
AD9236BCP-80EB	12-Bit, 80 MSPS ADC	
AD9432/PCB	12-Bit, 105 MSPS ADC	Rev. 0 Requires AD9432FFA
AD9433/PCB	12-Bit, 125 MSPS ADC	
AD9241-EB	14-Bit, 1.25 MSPS ADC	Requires AD922xFFA
AD9243-EB	14-Bit, 3 MSPS ADC	Requires AD922xFFA
AD9240-EB	14-Bit, 40 MSPS ADC	Requires AD922xFFA
AD9244-40PCB	14-Bit, 40 MSPS ADC	
AD9244-65PCB	14-Bit, 65 MSPS ADC	
AD6644ST/PCB	14-Bit, 65 MSPS ADC	Rev. C Requires AD664xFFA
AD9245BCP-80EB	14-Bit, 80 MSPS ADC	
AD6645/PCB	14-Bit, 80 MSPS ADC	Rev. C Requires AD664xFFA
AD9260-EB	16-Bit, 2.5 MSPS ADC	Requires AD922xFFA
AD10677/PCB	16-Bit, 65 MSPS ADC	Requires AD664xFFA
AD10678/PCB	16-Bit, 80 MSPS ADC	Requires AD664xFFA

Table 1

[1] Connector pin numbers and/or labeling on some evaluation boards (AD9214, AD9410, AD9430, AD9433, AD9235, and AD9244) may not match the FIFO connector numbering; however, the physical connections are correct.
[2] The AD6640 evaluation board has a 40-pin output connector that should be left (MSB) justified when connected to the 50-pin AD664x FIFO adapter.

THEORY OF OPERATION

The FIFO evaluation board can be divided into several circuits, each of which plays an important part in acquiring digital data from the ADC and allows the PC to upload and process that data. The evaluation kit is based around the IDT72V283 FIFO chip from IDT. This allows the system to acquire digital data at speeds up to 133 MSPS, up to data record lengths of 32K, using the HSC-ADC-EVAL-SC version of the FIFO evaluation kit. In order to allow dual ADCs or demultiplexed data from ADCs sampling faster than 133 MSPS to be evaluated with this system, two FIFO chips are available on the HSC-ADC-EVAL-DC version. Logic circuitry on the board and the ADC Analyzer software provided with the system allow for easy interfacing with the parallel port of a standard PC.

In operation, the FIFO chip(s) are given a specific amount of time to acquire a complete data record. The software will then start the read clock (RCLKA, RCLKB) which allows the PC to acquire the data record stored in the FIFO(s). Once data acquisition is complete, a master reset signal (MRS) is generated by the PC that resets the data address on the FIFO(s), starting the process over again.

The 16-bit data-words from the FIFO are acquired in 8-bit bytes by muxing the high and low eight bytes of the data onto the 8-bit data input of the parallel port. This is accomplished by connecting the high and low data bits directly via JP43–JP50 and controlling which bits appear on this bus via the buffer U2 and the signals GPPRD/$\overline{\text{GPPRD}}$ generated by the ADC Analyzer software.

The acquisition of data from FIFO 1 (U1) or FIFO 2 (U4) is controlled via the signals OEA and OEB, which originate in the ADC Analyzer software. Depending on which mode the ADC-EVAL system is operating in, OEA can be hardwired via JP26 or controlled via the ADC Analyzer through JP21.

Clocking Description

Each channel of the buffer memory requires a clock signal to capture the data. These clock signals are normally provided by the ADC evaluation board and are passed along with the data through Connector P1 (Pin 38 for Channel 1 and Pin 78 for Channel 2). If only a single clock is passed for both channels, they can be connected together by Jumper JP42.

The single-ended clock signal from each data channel is buffered and converted to a differential CMOS signal by two gates of a low voltage differential signal (LVDS) receiver, U3. This allows the clock source for each channel to be CMOS, TTL, or even ECL. The clock signals are ac-coupled by 0.1 µF capacitors: Jumper Position JP2 for Channel 1 and JP1 for Channel 2. Resistors R5, R7, and R2 for Channel 1 and R9, R24, and R10 for Channel 2 set the dc level at the input of U3 to approximately 1.2 V. Potentiometers R7 and R24 allow for fine-tuning the threshold of the LVDS gates. In applications where fine-tuning the threshold is critical, these potentiometers may be replaced with a higher resistance value to increase the adjustment range. Resistors R22 and R23 set the static input to each of these differential gates to a dc voltage of approximately 1.2 V.

At assembly, Jumpers JP7 and JP4 are both set to Position 1 or the noninverted output of each clock channel. This position is compatible with most devices, but Position 3 may be required for some ADCs. Please refer to Table 6 for the specific jumper settings recommended for each ADC evaluation board.

U17, an XOR gate array, is included in the design to allow users to add gate delays to the clock path to the FIFO memory chips. They are not required under normal conditions and are bypassed at assembly by Jumpers JP24 and JP31.

The clock paths described above determine the WRT_CLK1 and WRT_CLK2 signals at each FIFO memory chip (U1 and U4, Pin 80). The options above should allow the user to choose a clock signal that will meet the setup and hold time requirements (4 ns and 1 ns, respectively) to capture valid data.

Note that the user can apply a clock generator directly to S1 and/or S3. This clock generator should be the same unit that provides the clock for the ADC. These clock paths are ac-coupled, so a sine wave generator can be used. DC bias can be adjusted by R7/R24. Note that S1 and S3 (SMA connectors) are not installed at the factory and must be installed by the user.

The DS90LV048A differential line receiver is used to square the clock signal levels applied externally to the FIFO evaluation board. The output of this clock receiver directly drives the write clock of the IDT72V283 FIFO.

Clocking with Interleaved Data

ADCs with very high data rates may exceed the capability of a single buffer memory channel (~133 MSPS). These converters often demultiplex the data into two channels to reduce the rate required to capture the data. In these applications, the ADC Analyzer software must interleave the data from both channels to process it as a single channel. To accomplish this, the user can configure the software to process the first sample from Channel 1, the second from Channel 2, and so on. Or vice versa, the first sample from Channel 2, the second from Channel 1, and so on (see the Troubleshooting section for more information). The synchronization circuit included in the buffer memory (see the PCB schematics in Figure 28–Figure 33) forces a small delay between the write enable signals (WENA and WENB) to the FIFO memory chips (Pin 1, U1 and U4), ensuring that the data from Channel 1 is captured first.

USING ADC ANALYZER SOFTWARE

The ADC Analyzer software is designed to make it easy to quickly evaluate the performance of an Analog Devices analog-to-digital converter.

Installation

Note that a copy of the ADC Analyzer software is included on the CD with the FIFO Evaluation Kit. Please check the Analog Devices website for updates to the software at www.analog.com/hsc-FIFO.

1. Copy the AnalyzerSetup.exe file to the hard drive.

2. Run the executable file and follow the instructions given in the installation wizard. Note that administrator privileges are required to install the software on Windows 2000/Windows NT machines.

3. Once the software is installed, run the executable file (the default location is in C:\Program Files\ADC_Analyzer\ADC_Analyzer.exe).

Configuration File

A configuration file can be created for each high speed ADC evaluation board used with the ADC Analyzer software. This file provides the software with important information about the data sent from the ADC evaluation board to the FIFO evaluation board, such as the number of bits, speed of the clock, and format of the data bits (binary or twos complement). Configuration files for some of the evaluation boards are included with the ADC Analyzer software files. Each time the ADC Analyzer software is opened a window will appear in which a configuration file can be specified. Click Yes to specify a configuration file and choose the file corresponding to the ADC evaluation board being used.

The default configuration files can be modified or a new configuration file can be created using the following instructions.

Configuring an Evaluation Board

Follow these steps to configure the software with the ADC evaluation board:

1. From the pull-down menus in the upper left hand corner, choose Config>DUT. A screen similar to Figure 3 will appear. Type the name of the ADC being evaluated in the Device box and the number of bits (resolution of the ADC) in the Number of Bits box. (Note: This information is only used for display purposes.) To specify a directory different from the default to store the configuration file, type a new location in the Default Data Directory box and then click OK.

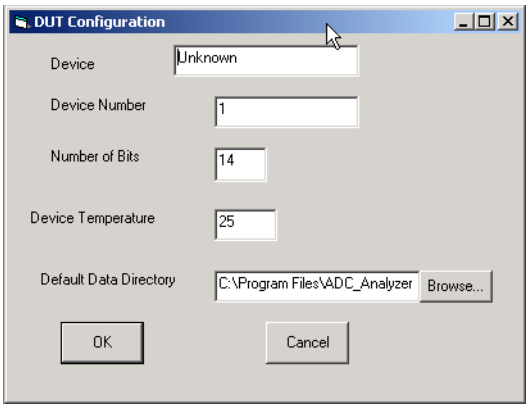


Figure 3. DUT Configuration

2. Next, choose Config>FFT from the pull-down menus. In this window, configure the Fast Fourier Transform plot (see Figure 4). If evaluating a single ADC or a demultiplexed ADC, modify the options under Channel A. If evaluating a dual ADC, modify the options under both channels. After configuring the options in this window, click OK.

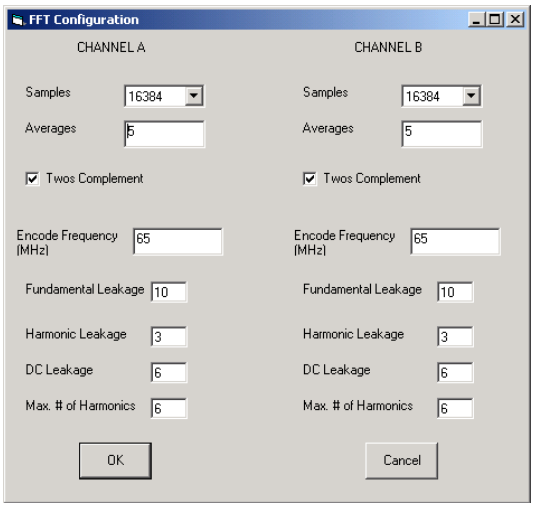


Figure 4. FFT Configuration

Note that Channel A in the software corresponds to Channel 1 on the FIFO schematics and the bottom FIFO on the evaluation board. Channel B corresponds to Channel 2 on the FIFO schematics and the top FIFO on the evaluation board (closest to the Analog Devices logo). See the Jumpers section for more information.

Below are descriptions of the available options.

Samples: Choose the number of samples taken to calculate an FFT. The default is 16K samples. Users can choose more or fewer samples, depending on the application. The maximum number of samples that can be selected in the software is 256K. However, the FIFO evaluation boards are configured with 32K FIFOs. For single ADCs evaluated with the HSC-ADC-EVAL-SC model, the maximum number of samples selected should match the FIFO memory on the evaluation board. For dual ADCs evaluated with the HSC-ADC-EVAL-DC model, the maximum number of samples should match the FIFO memory of each channel (a different number of samples can be selected for each channel). ADCs with demultiplexed outputs (such as the AD9430) can be used with a sample value of twice the FIFO memory. See the Upgrading FIFO Memory section for more information.

Averages: Specify the number of averages taken for the average FFT functions. See the ADC Analyzer Software Functions section for more information.

Twos Complement: Check this box if the data from the ADC evaluation board is in twos complement format. Refer to the ADC data sheet to determine if the ADC outputs are configured for twos complement or binary data.

Encode Frequency (MHz): Enter the speed of the encode clock to the ADC. If evaluating a dual ADC, two different clock rates can be entered.

Fundamental Leakage: The number of bins around the fundamental signal used in calculating the SNR and SINAD. The type of windowing selected determines the default value of the fundamental leakage. See the Windowing section for more information. The default values are 25, 10, and 0 for Hanning, Blackman Harris, and no windowing, respectively.

Harmonic Leakage: The number of bins around the harmonics of the fundamental signal. These are used in calculating SNR and SINAD. Typically, this can be left at the default value of 3.

DC Leakage: The number of bins (at dc) that are not used in calculating SNR and SINAD. Typically, this can be left at the default value of 6.

Maximum Number of Harmonics: The number of harmonics displayed by the ADC Analyzer. The default value is 6 and the maximum number of harmonics that can be displayed is 10.

3. Next, choose Config>Buffer. A window similar to Figure 5 will appear.

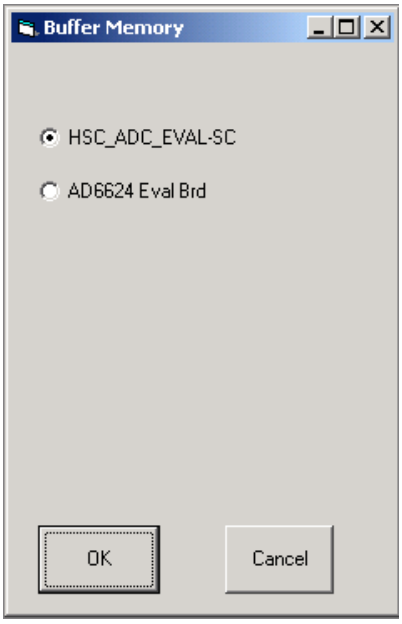


Figure 5. Buffer Memory

HSC-ADC-EVAL-SC should be selected. Click OK and the window in Figure 6 will appear. Choose the appropriate parallel port and click OK.

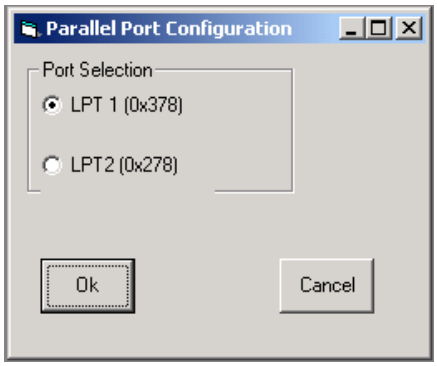


Figure 6. Parallel Port Configuration

4. Next, choose Config>Bits>Data Bits. Configure the number and location of the data bits used to calculate the FFTs. Make sure the number of bits matches the resolution of the converter. All of the supported evaluation boards are MSB justified, so check the number of bits for the converter starting with Bit 15 (MSB). Exceptions to this are the AD9280, AD9281, AD9200, and AD9201. For these four ADCs, check the number of bits starting with Bit 13. If a single ADC is being evaluated,

check only Channel A and the appropriate bits under Channel A. If a dual ADC is being evaluated, check Channel A and Channel B. If a demultiplexed ADC is being evaluated, check the Interleaved Data box. This automatically selects both Channel A and Channel B (see Figure 7).

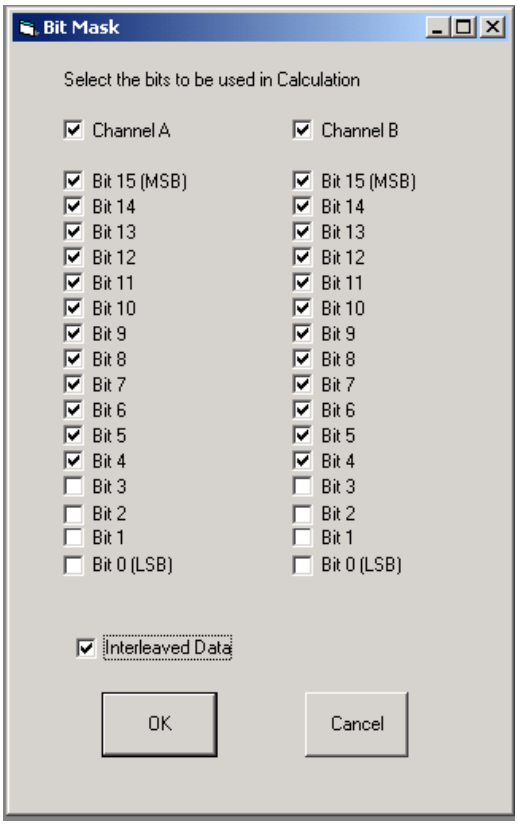


Figure 7. Bit Mask Configuration

If the Interleaved Data box is selected, the window in Figure 8 will appear once OK is clicked.

Figure 8. Interleaved Priority

Note that Channel A in the software corresponds to Channel 1 on the FIFO schematics and the bottom FIFO on the evaluation board. Channel B corresponds to Channel 2 on the FIFO schematics and the top FIFO on the evaluation board (closest to the Analog Devices logo). See the Jumpers section for more information.

Click OK. See the Troubleshooting section for more information about this window.

5. Finally, choose File>Configuration File>Save Configuration from the pull-down menu to save the configuration for future use. Choose a file name and a location to save the file.

Additional Configuration Options

Other options under the configuration pull-down menu include Windowing, Power Supply, and Y-Axis.

WINDOWING

Choose either the Hanning or Blackman Harris (default) windowing functions or turn windowing off. See the Windowing Functions section for a description of Hanning and Blackman Harris windowing. Click OK. If none is selected, a Coherent Sampling Calculator will appear (see Figure 10).

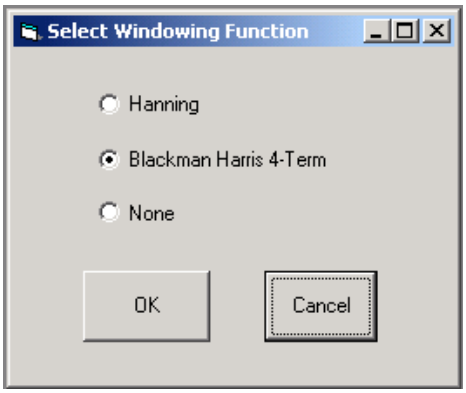


Figure 9. Windowing Function Selection

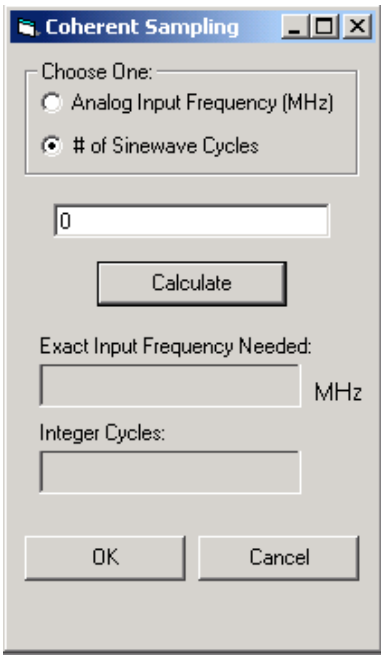


Figure 10. Coherent Sampling Calculator

For the calculator to work properly, the correct sampling frequency must be entered under Config>FFT. Enter either the desired approximate Analog Input Frequency or the Number of Sine Wave Cycles. Enter the value in the white box and click on Calculate to view the Coherent Frequency. The Coherent Frequency and Number of Integer Cycles will be displayed in the gray boxes. Click OK to exit the Coherent Sampling Calculator.

POWER SUPPLY

Under this option, users type in the value of the ADC analog and digital voltage supplies (see Figure 11). The ADC Analyzer will display this information, along with other values, when data is captured. See the ADC Analyzer Software Functions section for more information.

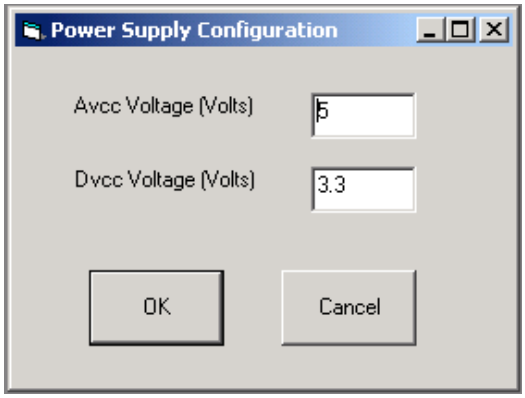


Figure 11. Power Supply Configuration

Y-AXIS

This box can be used to configure the display of the FFT Y-Axis. The default value of –130 is a typical setting for the noise floor of a 14-bit ADC with 16,384 samples in the FFT calculation.

Figure 12. Y-Axis Configuration

ADC ANALYZER SOFTWARE FUNCTIONS

A number of functions can be performed on the data collected by the FIFO evaluation board. These functions are represented by the row of buttons under the pull-down menu. The same functions can also be accessed under the Analyze pull-down menu. A description of each of the buttons is listed below.

TIME DOMAIN

This function displays a reconstruction of the captured data and is a useful troubleshooting tool. For example, the time-domain plot can help track down timing and data capture issues. Several values are listed to the left of the signal, including:

AVCC: Analog voltage level, set under Config>Power Supply (for display purposes only)

DVCC: Digital voltage level, set under Config>Power Supply (for display purposes only)

Encode: ADC clock rate (MSPS)

Analog: Calculated analog input frequency (MHz). In IF sampling applications, the analog input is calculated back to the first Nyquist zone.

Min: Minimum output code produced by the analog input

Max: Maximum output code produced by the analog input

Range: The range of the codes produced by the analog input

Average: Average value of the codes; may be interpreted as the common mode

FS: Full-scale code range, equal to 2^n where n is the number of bits

Samples: Number of samples taken, determined by FFT Configuration (Config>FFT)

CONTINUOUS TIME DOMAIN

This function displays a continuous reconstruction of the captured data and is also useful for trouble–shooting. Click on the STOP button to end the continuous display.

FFT

When the FFT graph is selected, a similar window opens with the following data:

AVCC: Analog voltage level, set under Config>Power Supply (for display purposes only)

DVCC: Digital voltage level, set under Config>Power Supply (for display purposes only)

Encode: ADC clock rate (MSPS)

Analog: Calculated analog input frequency (MHz). In IF sampling applications, the analog input is calculated back to the first Nyquist zone.

SNR: Signal-to-noise ratio (dB)

SNRFS: Signal-to-noise ratio full scale (dBFS)

SINAD: Signal-to-noise plus distortion (dB)

Fund: Level of the fundamental (highest) tone (dBFS)

Second: Level of the second harmonic (dBc) of the fundamental

Third: Level of the third harmonic (dBc) of the fundamental

Fourth: Level of the fourth harmonic (dBc) of the fundamental

Fifth: Level of the fifth harmonic (dBc) of the fundamental

Sixth: Level of the sixth harmonic (dBc) of the fundamental

WoSpur: Level of the worst (nonharmonic) spur

THD: Total harmonic distortion (dBc)

SFDR: Spurious-free dynamic range (dBc)

Noise Floor: Level of the noise floor (dBFS)

Samples: Number of samples taken, determined by FFT Configuration (Config>FFT)

CONTINUOUS FFT

This function displays a continuous FFT.

AVERAGE FFT

This functions displays an average of a user-specified number of FFTs. Configure the number of FFTs under Config>FFT. The default value is 5.

CONTINUOUS AVERAGE FFT

This function displays a continuous average of a user-specified number of FFTs. Configure the number of FFTs under Config>FFT. The default value is 5.

TWO TONE

This function is used to analyze dual-tone analog inputs.

AVCC: Analog voltage level, set under Config>Power Supply (for display purposes only)

DVCC: Digital voltage level, set under Config>Power Supply (for display purposes only)

Encode: ADC clock rate (MSPS)

Analog 1: First analog input frequency (MHz)

Analog 2: Second analog input frequency (MHz)

Fundamental 1: First fundamental tone (dBFS)

Fundamental 2: Second fundamental tone (dBFS)

F1 + F2: Sum of the fundamental tones (dBFS)

F2 – F1: Difference of the fundamental tones (dBFS)

2F1 – F2: 2 × Fundamental 1 – Fundamental 2 (dBFS)

2F1 + F2: 2 × Fundamental 1 + Fundamental 2 (dBFS)

2F2 – F1: 2 × Fundamental 2 – Fundamental 1 (dBFS)

2F2 + F1: 2 × Fundamental 2 + Fundamental 1 (dBFS)

WoIMD: Worst intermodulation distortion (dBc)

SFDR: Spurious-free dynamic range (dBc)

Noise Floor: Level of the noise floor (dBFS)

Samples: Number of samples taken, determined by FFT Configuration (Config>FFT)

CONTINUOUS TWO TONE

This function displays a continuous dual-tone FFT.

AVERGAGE TWO TONE

This function displays an average of a user-specified number of dual-tone FFTs. Configure the number of FFTs under Config>FFT. The default value is 5.

STOP

Click on this button to end any of the continuous display functions.

ZOOMING AND EXPORTING DATA

To zoom in on any portion of a displayed analog signal or FFT, select the portion of the signal by holding down the left mouse button and dragging across the area of interest. Bring up a hidden menu by clicking the right mouse button in the active window. The hidden menus are slightly different for the time-domain and FFT plots. These hidden menus have several options, including zooming and the capability to export time-domain data (see Figure 18 and Figure 19). Select from the menus using the left mouse button (see Figure 13 and Figure 14).

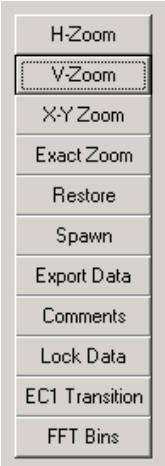


Figure 13. Time-Domain Plot Hidden Menu

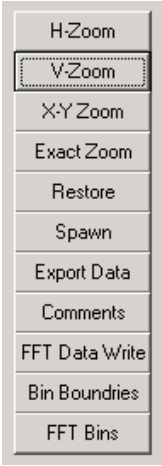


Figure 14. FFT Plot Hidden Menu

H-Zoom: Scales the selected section horizontally.

V-Zoom: Scales the selected section vertically.

X-Y Zoom: Scales horizontally and vertically (two dimensions).

Exact Zoom: Enter specific coordinates to view.

Restore: Restores the graph to its original view.

Spawn: Produces an exact working copy of the active window that can be analyzed separately

Export Data: Writes all of the data points as well as the calculated information to a file. The information is saved as a .csv file that can be viewed in Excel.

Comments: Allows the user to enter comments about the graph. If the FFT is printed, the comments will be included in the printout.

Lock Data (Time-Domain Plot Only): Once a time-domain sample of the data is taken, the user can "lock" this data and then perform an FFT. The FFT will be calculated based on this data instead of a new sample of data.

FFT Data Write (FFT Plot Only): Writes the calculated data to a file.

Bin Boundaries (FFT Plot Only): Highlights the bins used to calculate the fundamental and harmonic energy. Configure the Fundamental Leakage and Harmonic Leakage under Config>FFT. See the Configuring an Evaluation Board section for more information.

FFT Bins: Changes the X-axis of the graph from frequency to bins.

IMPORTING DATA

Data can be imported into the ADC Analyzer so that an FFT calculation can be performed on the data. Two types of data can be imported: raw text data in decimal format (from a logic analyzer, for example) and data exported from the ADC Analyzer.

To import data previously exported from the ADC Analyzer:

1. Choose File>Import Data in the software.
2. Type the file path in the dialog box shown in Figure 15 or click on the Browse… button to search for the file. Click OK.
3. The time-domain data will be graphed in a new window. Right click on the graph to bring up the hidden menu. Select Lock Data from the menu.
4. Click on the FFT button to perform an FFT on this data.

To import raw text data in decimal format:

1. Choose File>Import Data in the software.
2. Click on the ASCII File button shown in Figure 15.
3. The window in Figure 16 will appear. This window is used to give ADC Analyzer information about how to interpret the text data file.

   Data Bits: Select the resolution of the ADC.

   Samples: Select the number of samples in the file.

   Data Format: Select the format of the ADC output data.

   Justification: Normally, LSB_Justified should be selected. This means the data point is the true code (for example, 0, 1, 2, … 16,383 for a 14-bit converter). Data exported from the ADC Analyzer is MSB_Justified, meaning the data has been multiplied by a factor.

   Encode Frequency (MHz): Type in the clock sampling rate used.

   ASCII Text File to Import: Click the Browse button to search for the file.

4. Click OK. The time-domain data will be graphed in a new window. Right click on the graph to bring up the hidden menu. Select Lock Data from the menu.
5. Click on the FFT button to perform an FFT on this data.

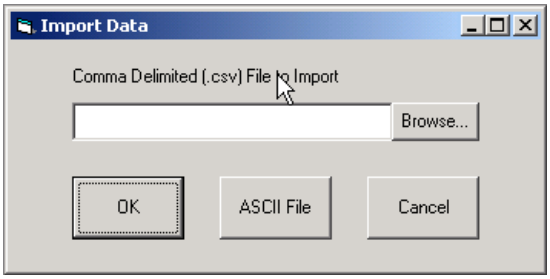


Figure 15. Import Data Dialog Box

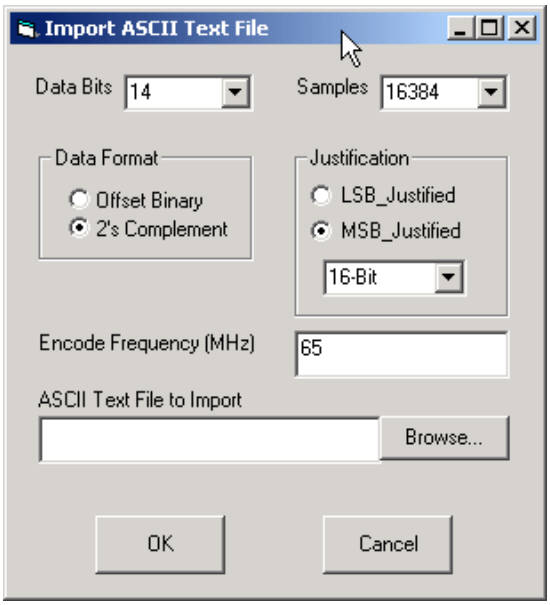


Figure 16. Import ASCII Text File Dialog Box

PRINTING

There are several printing options available in the ADC Analyzer. To print the active window, choose File>Print >Print Active. To print more than one open window, choose File>Print>Print List. A dialogue box will display in which the user can choose which windows to print. Choose multiple windows by clicking on each window while pressing the CTRL key or print all open windows with the Print All button. Finally, to print the entire screen, choose File>Print>Print Screen.

SAVING FILES

There are three ways to save an image as a bit map file from the ADC Analyzer. Choose File>Save As>Save Active to save the active window in bit map or jpeg format. Choose File>Save As>Save List to save each open window as a separate bit map file. Finally, choose File>Save As>Save Screen to save the entire screen as a bit map file.

COHERENT SAMPLING

In order for the system to be defined as coherent, the analog and encode source must be synchronized, and the analog and encode input frequencies must be selected such that with a sample size of 2^N (N is an integer number) there is an integer number of whole sine wave cycles. Additionally, the number of cycles should ideally be a prime number. Selecting a prime number ensures that the same converter codes are not repeated over and over, exercising as many of the converter codes as possible. Although a crystal oscillator can be used as an encode source in this technique, two synchronized signal synthesizers are generally preferred because special hardware may be required to ensure the crystal oscillator is synchronized with the analog source. The following equation can be used to mathematically calculate the correct analog and encode frequencies for a coherent system:

$$\frac{fin}{fs} = \frac{M}{Mc}$$

where:

fin = Analog Input Frequency

fs = Encode Frequency

M = Sample Size (2^N)

Mc = Number of Cycles of Sine Wave

If the requirements of the coherent system defined above are not met, the discrete time samples will appear discontinuous at the end of the captured samples and the results will be invalid.

WINDOWING FUNCTIONS

Because coherent sampling has strict requirements for the analog and encode source, it is sometimes desirable to use a windowing function instead. There are many windowing functions available, but two of the most popular are the Blackman Harris 4-Term and the Hanning window. With windowing, the time-domain samples are multiplied by the appropriate weighting function that weights the time-domain data such that the discontinuities at the end of the captured samples have less significance.

The weighting function for a Blackman Harris 4-Term window is:

$$Wn = a0 - a1 \times \cos\left(\frac{2\pi \times n}{M}\right) + a2 \times \cos\left(\frac{2\pi \times 2n}{M}\right) - a3 \times \cos\left(\frac{2\pi \times 3n}{M}\right)$$

where:

$a0$ = 0.35875

$a1$ = 0.48829

$a2$ = 0.14128

$a3$ = 0.01168

M = Sample Size (2^N)

n = Indexed Sample Number

The weighting function for a Hanning window is:

$$Wn = 0.5 - 0.5 \times \cos\left(\frac{2\pi \times n}{M}\right)$$

where:

M = Sample Size(2^N)

n = Indexed Sample Number

FFT CALCULATIONS

Whether a system is coherent or a windowing function has been applied, the resulting data will be processed via a discrete fourier analysis that translates the discrete time-domain samples into the frequency domain. Because in practice processing the data quickly is desired, a Fast Fourier Transform (FFT) is used, which is simply an algorithm that reduces the required mathematical calculations. There are many FFT algorithms available but the most popular is the radix 2 algorithm. Regardless of the algorithm, for each time-domain sample a complex conjugate pair ($r \pm jx$) will be generated from the FFT. For example, if the time-domain sample size is 16,384, the resulting FFT array will contain 163,384 complex samples. In order to generate a frequency domain plot from this data, the magnitude of each complex sample must be calculated. The magnitude can be computed using the following equation:

$$Magnitude = \sqrt{Re^2 + Im^2}$$

If the input data to the FFT is complex, then the FFT will contain 16,384 magnitudes representing frequencies between plus and minus $fs/2$. Although "complex" ADCs are not available, it is very common to use two ADCs to synchronously sample the I and Q data streams from a quadrature demodulator. If the data input to the FFT is real, representing the data from a single ADC, the last 8192 samples represent a mirror image of the first 8192 samples. Because this is an exact mirror image, the last 8192 samples can be ignored.

With the data set processed, there are two ways to evaluate the ADC performance, graphically and computationally. In order to plot the data in a meaningful way, the magnitude data must be converted to decibels (dB). This can be done with the formula:

$$dB = 10 \times \log_{10}\left(\frac{Magnitude}{Magnitude_{Max}}\right)$$

where *Magnitude* is the individual array elements computed above,

and $Magnitude_{max}$ is the maximum magnitude element in the array. It is important to note that the computation for *dB* assumes the square root was not actually taken in the equation above, leaving the magnitude expressed as the sum of two squares. Therefore 10 × log is used instead of 20 × log, thus eliminating the time required to compute the square root.

Based on the Nyquist Theory, the sample rate must be at least twice the signal bandwidth to faithfully represent the signal when sampled. Therefore, if the sample rate is 80 MHz, an ADC can only represent 40 MHz of continuous bandwidth. Knowing the sample rate and the number of time-domain samples, the frequency representation per bin can be established. In this example, the sample rate is 80 MHz and there are 16,384 time-domain samples; therefore, 4880 Hz/bin is represented. If the sample rate is doubled or the number of time-domain samples is doubled, a 3 dB improvement in the noise floor will be observed. This does not represent an improvement in ADC performance but simply represents an increased resolution per bin.

From the computations above, it is now possible to define and calculate SNR, SINAD, harmonics, SFDR, ENOB, and noise figure. The signal-to-noise ratio can be expressed as the ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first six harmonics and dc, or by the equation:

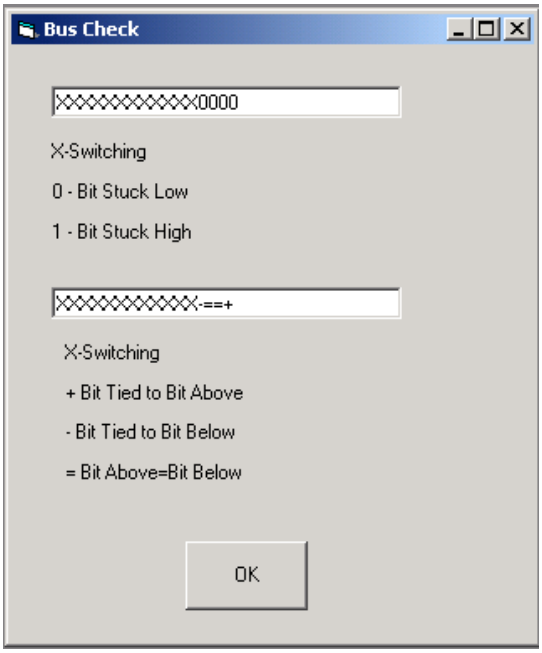
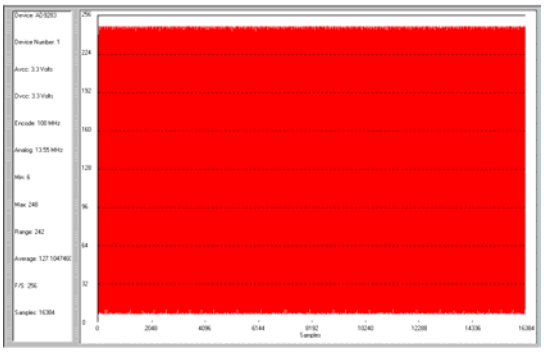
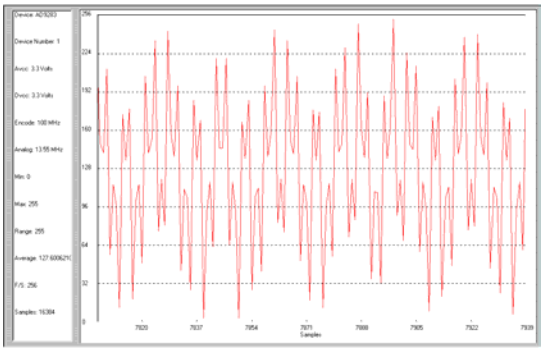
$$SNR = 20 \times \log_{10}\left(\frac{Fundamental\_Energy}{Noise\_Energy}\right) dB$$

The *Noise_Energy* represents the summation of all the noise energy in the spectrum, and the *Fundamental_Energy* represents the summation of the fundamental energy. The fundamental energy will reside in a single bin if a coherent system is used; however, in the case of a windowing function, it may be spread over 10 to 25 bins, depending on the windowing technique.

Correspondingly, harmonics can be defined as the ratio of the rms signal amplitude to the rms value of the harmonic component, reported in dBc. Harmonics represent the nonlinearities within the ADC and are integer multiples of the fundamental. If the harmonic exceeds *fs*/2, it will be aliased back into the first Nyquist zone. A concept closely related to harmonics is SFDR. For an ADC, SFDR is defined as the ratio between the rms amplitude of a single tone and the rms amplitude of the worst spur as the tone is swept through the entire ADC input range. It is very common for the worst spur to be harmonically related.

Whereas SNR excludes the first six harmonics, SINAD includes these harmonics as part of the *Noise_Energy* summation. If the harmonic performance of the ADC is excellent, there will be very little difference between the SNR value and the SINAD value.

TROUBLESHOOTING

Scenario	Troubleshooting	Screenshot
After clicking on the time data button, the signal displayed in the window is a flat line.	1. Check the power connections. 2. Verify that the parallel printer cable is IEEE-1284 compatible. 3. Check the printer cable connection between the PC and the FIFO board. Ensure the correct parallel port is selected (LPT1 or LPT2) under Config>Buffer. 4. Make sure the Printer Port in the computer's BIOS is set to "Standard Bidirectional." 5. Make sure Channel A, Channel B, or both channels are selected under Config>FFT. 6. Check the signal connections and make sure the encode clock is present at the output of the A/D evaluation board. 7. Verify that data bits are switching at the connection point between the FIFO and the ADC evaluation board. 8. Use the Analyze>Bus Check option to ensure all data bits are switching (see Figure 17). The left-most bit is the MSB. 9. Use the ADC data sheet to ensure all jumper connections are set appropriately on the ADC evaluation board. Ensure the ADC's power-down option is not active. 10. Refer to Table 4 to ensure that all jumpers are set appropriately.	 *Figure 17. Bus Check for a 12-Bit ADC*
After clicking on the time data button, the signal displayed does not look like the analog input signal.	1. A fast sinusoidal signal may look like a solid red block in the time-domain window (due to the number of sine waves shown). Right click on the window to bring up a hidden menu where you can zoom in to a closer view of the signal. 2. Check the printer cable connection between the PC and the FIFO board. Ensure the correct parallel port is selected (LPT1 or LPT2) under Config>Buffer. 3. Check the signal connections. 4. Use the Analyze>Bus Check option to ensure all of the data bits are switching. 5. Ensure that the Twos Complement button is set correctly under Config>FFT. If the Twos Complement box is checked and the ADC outputs are not in twos complement format, a time-domain plot may look like Figure 19. 6. Adjust the timing to ensure that the data is captured correctly. Refer to the Clocking Description section and Table 4 for more information. 7. Try using a very low frequency analog input (for example, 100 kHz) to debug timing issues. 8. Check for problems with the common-mode level by looking at the time data with no analog input signal.	 *Figure 18. Typical Time Domain Plot*  *Figure 19. Incorrect Setting for Twos Complement (Horizontal Zoom)*

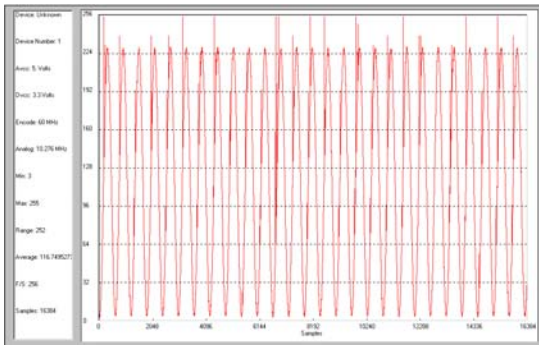
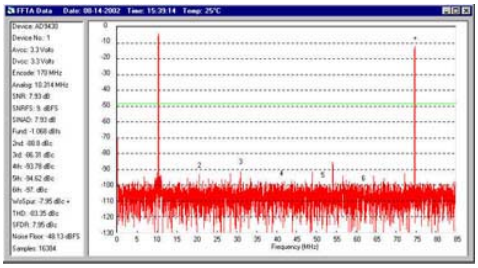
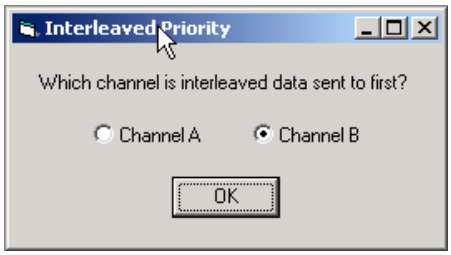
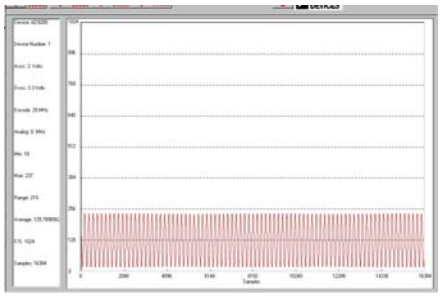
Scenario	Troubleshooting	Screenshot
The noise floor of the FFT is higher than expected.	Note that a higher than expected noise floor on the FFT can often be traced back to timing issues in the clock path. If this is suspected, the user should try the following: 1. Put a very slow sine wave signal into the ADC (such as 100 kHz) and initiate a time-domain plot. If the plot looks similar to Figure 20, there are timing issues. 2. Switch Jumpers JP4 and/or JP7 to their alternate positions. 3. The four XOR gates of U17 can be used to insert delay into the high speed clock path or to invert the clock in order to optimize timing. With U17 in place, Jumpers JP2 and JP31 can be unsoldered and the Jumper pairs JP27 and JP30 or JP28 and JP29 can be soldered in place. This should allow enough flexibility for the user to adjust timing under any conditions.	 *Figure 20. Timing Issues*
There is a large spur in the FFT (image of the fundamental) when evaluating the AD9430.	1. Click Config>Bits>Data Bits. When the Bit Mask window (Figure 7) appears, click OK. The window in Figure 22 will appear. Select Channel B if Channel A is selected (or select Channel A if Channel B is selected). Click OK. Note that Channel A in the software corresponds to Channel 1 on the FIFO schematics and the bottom FIFO on the evaluation board. Channel B corresponds to Channel 2 on the FIFO schematics and the top FIFO on the evaluation board (closest to the Analog Devices logo). See the Jumpers section for more information. 2. Perform another FFT. The spur should disappear.	 *Figure 21. AD9430 Timing Issue*  *Figure 22. Interleaved Priority*
The two MSBs are missing from the time-domain plot.	1. If evaluating the AD9280, AD9281, AD9200, or AD9201, make sure the appropriate bits are selected under Config>Bits>Data Bits. Bits 13–6 should be selected for the AD9280 and AD9281. Bits 13–4 should be selected for the AD9200 and AD9201. Default configuration files for these ADCs are installed with the ADC Analyzer. 2. Make sure the bits are switching at the FIFO connector.	 *Figure 23. Incorrect Bit Mask Setting*

Table 2. Troubleshooting

Upgrading FIFO Memory

The FIFO evaluation board includes one or two 32K FIFOs, depending on the model. Pin compatible FIFO upgrades (64K to 256K) are available from Integrated Device Technology, Inc. (IDT). The IDT part numbers are:

- IDT72V283: 32K (included)
- IDT72V293: 64K
- IDT72V2103: 132K
- IDT72V2113: 256K

For more information, visit www.idt.com

BILL OF MATERIALS

Item	Quantity		Reference Designation	Description	Package	Value
	SC	DC				
1	3	3	C1, C27, C28	Capacitor		10 µF
2	27	27	C2–C7, C9–C10, C12–C15, C18–C26, C29–C33, C39	Capacitor	1206	0.1 µF
3	2	2	C8, C34	Capacitor		0.1 µF
4	2	2	C16, C17	Capacitor	1206	330 pF
5	4	4	C35–C38	Capacitor	0603	0.1 µF
6	2	2	JP1–JP2	Capacitor		0.1 µF
7	16	16	JP3, JP19–JP21, JP25–JP26, JP34–JP41	2-Pin Jumper Head		
8	4	4	JP4–JP7	3-Pin Jumper Head		
9	25	25	JP8–JP15, JP22–JP24, JP27–JP31, JP42–JP50	Solder Bridge (No Component)		
10	5	5	JP16–JP18, JP32–JP33	Solder Bridge (No Component)		
11	1	1	P1	80-Pin RA Header	Female	
12	1	1	P2	Printer Cable Connector		552742-1
13	0	0	P3	68-Pin Plug RA (Not Populated)		2-174225-5
14	0	0	PR1–PR2	Probe Connector		
15	2	2	R1, R19	Resistor	1206	220 Ω
16	3	3	R5, R9, R22	Resistor	1206	2 kΩ
17	2	2	R3–R4	Resistor	1206	10 kΩ
18	0	0	R44	Resistor (Not Populated)	1206	1 kΩ
19	2	2	R6, R29	Resistor	1206	1 kΩ
20	2	2	R7, R24	Potentiometer		100 Ω
21	0	0	R8, R20, R27, R28	Resistor (Not Populated)	1206	
22	5	5	R11–R13, R30–R31	Resistor	1206	1 kΩ
23	6	6	R14–R18, R21	Resistor	1206	1.5 kΩ
24	4	4	R2, R10, R23, R25	Resistor	1206	1.2 kΩ
25	1	1	R26	Resistor	1206	1.8 kΩ
26	8	8	R32, R34, R36–R37, R39–R40, R42, R43	Resistor	1206	150 Ω
27	4	4	R33, R35, R38, R41	Resistor	1206	136 Ω
28	0	0	S1, S3	SMA Connector RF 5-Pin Upright (Not Populated)		
29	1	1	TB1	Power Connector		Wieland 25.602.2352.0, 25.530.0325.0
30	2	2	TP1, TP2	Pin Cup		
31	1	2	U1, U4	32K FIFO	TQFP-80	IDT 72V283
32	1	1	U2	16-Bit Line Driver	SSOP-48	74ACT16541
33	1	1	U3	Quad Differential Line Receiver	SOIC-16	DS90LV048A
34	3	3	U5, U11, U14	Quad 2-Input NAND Gate	SOIC-14	74AC00
35	2	2	U6, U9	ECL D-Type Flip-Flop	SOIC-8	MC100EP31
36	1	1	U7	Dual D-Type Flip-Flop	SOIC-14	74AC74
37	1	1	U10	Dual LVTTL/LVCMOS to Differential LVPECL Translator	SOIC-8	MC100EPT22
38	2	2	U12–U13	Octal D-Type Flip-Flop	SOIC-20	74AC574
39	1	1	U15	Quad 2-Input OR Gate	SOIC-14	74AC32
40	1	1	U16	Dual Differential PECL to TTL Translator	SOIC-8	MC100EPT23
41	1	1	U17	Quad 2-Input XOR Gate	SOIC-14	74VCX86

Table 3. HSC-ADC-EVAL-SC/HSC-ADC-EVAL-DC Bill of Materials

JUMPERS

Below is the orientation in which the FIFO evaluation board should be held in order to configure the jumpers. Use the following legend to configure the jumpers: Channel 1 is associated with the bottom IDT FIFO chip, and Channel 2 is associated with the top IDT FIFO chip (closest to the Analog Devices logo).

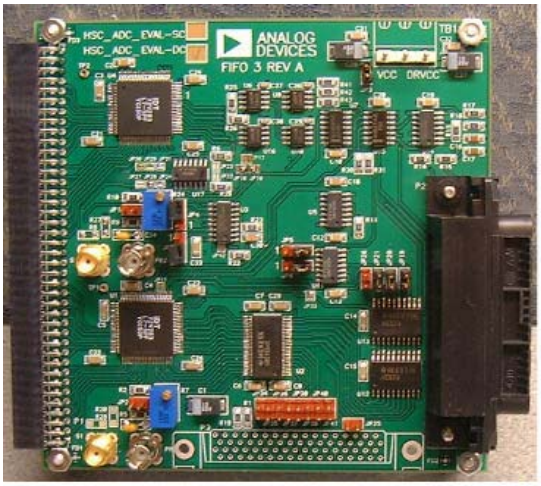


Figure 24. FIFO Evaluation Board Orientation (Front)

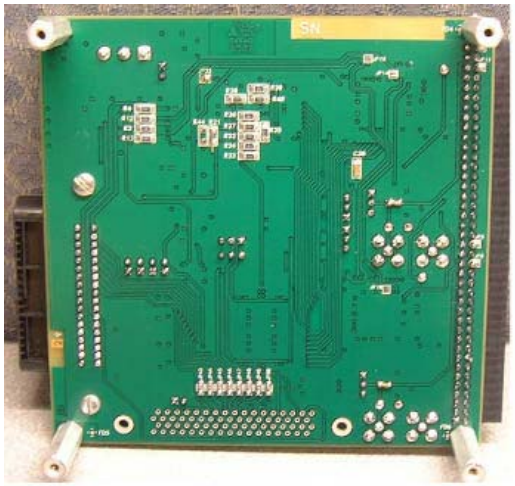


Figure 25. FIFO Evaluation Board Orientation (Back)

Use the following legend to configure the jumpers.

Position	Description
In	Jumper in place (2-pin header)
Out	Jumper removed (2-pin header)
Position 1 or Position 3	Denotes the position of a 3-pin header. Position 1 is marked on the board.

Table 4. Jumper Legend

Position	Description
In	Solder pads should be connected
Out	Solder pads should not be connected
Up	Upper two solder pads should be connected
Down	Lower two solder pads should be connected
Left	Left two solder pads should be connected
Right	Right two solder pads should be connected

Table 5. Solder Bridge Legend

Default Settings

Below are the default settings for each model of the FIFO Evaluation Kit. The –DC model is configured to work with demultiplexed ADCs (such as the AD9430). Dual ADC settings are shown in a separate column. Some evaluation boards may require modifications to these settings to properly align the timing. Refer to the Clocking Description section for more information.

Jumper Configuration

Jumper No.	Solder Bridge	SC Default	DC Default	Dual Settings	Description
JP1					Not used: a 0.1 µF capacitor is soldered across this jumper
JP2					Not used: a 0.1 µF capacitor is soldered across this jumper
JP3		In	In	In	Connects DRVCC to VCC, allowing the FIFO board to run on a single 3 V supply
JP4		Position 3	Position 1	Position 1	Allows delays to be added to the clock paths 1: Noninverted output of clock channel 3: Inverted output of clock channel
JP5		Position 3	Position 3	Position 3	Software configuration—no adjustment needed
JP6		Position 3	Position 3	Position 3	Software configuration—no adjustment needed
JP7		Position 3	Position 1	Position 1	Allows delays to be added to the clock paths 1: Noninverted output of clock channel 3: Inverted output of clock channel
JP8	✓	In	In	In	Connects Pin 36 of the P1 header to ground
JP9	✓	In	In	In	Connects Pin 40 of the P1 header to ground
JP10	✓	Out	Out	Out	Takes the FF signal on FIFO1 out of the circuit
JP11	✓	Out	Out	Out	Takes the EF signal on FIFO1 out of the circuit
JP12	✓	In	In	In	Connects Pin 80 of the P1 header to ground
JP13	✓	In	In	In	Connects Pin 76 of the P1 header to ground
JP14	✓	Out	Out	Out	Takes the FF signal on FIFO2 out of the circuit
JP15	✓	Out	Out	Out	Takes the EF signal on FIFO2 out of the circuit
JP16	✓	Left	Left	Left	The direction in which JP16 and JP18 are soldered allows the WEN signal on the FIFO board to drive FIFO1 and FIFO2 (WENA and WENB) directly or allows the synchronization circuit to generate WENA and WENB from the WENS signal generated by the PC (default)
JP17	✓	Left	Left	Left	Determines which data channel is first when interleaving the incoming data (used with ADCs that have demultiplexed outputs)
JP18	✓	Right	Right	Right	The direction in which JP16 and JP18 are soldered allows the WEN signal on the FIFO board to drive FIFO1 and FIFO2 (WENA and WENB) directly or allows the synchronization circuit to generate WENA and WENB from the WEN signal generated by the PC (default)
JP19		In	In	In	Allows the PC to control the MRS and RCLKA/RCLKAB signals
JP20		In	In	In	Allows the PC to control the MRS and RCLKA/RCLKAB signals
JP21		In	In	In	For use with the ADC Analyzer. When inserted, allows the dual-mode FIFO read back (generated by the PC) to select either FIFO1 or FIFO2 when acquiring data from the FIFO board.
JP22	✓	Out	Out	Out	Switches XOR gate in FIFO clock path between invert and pass-through
JP23	✓	Out	Out	Out	Switches XOR gate in FIFO clock path between invert and pass-through
JP24	✓	In	In	In	Bypasses two additional gate delays to the clock path (WRT_CLK1)
JP25		Out	Out	Out	Software configuration – no adjustment needed
JP26		Out	Out	Out	For use with the two FIFOs installed. This allows the user to manually switch the FIFO data being acquired to FIFO1 (jumper removed) or FIFO2 (jumper inserted).
JP27	✓	Out	Out	Out	Used to insert additional gate delays to the clock path
JP28	✓	Out	Out	Out	Bypasses one gate delay to the clock path
JP29	✓	Out	Out	Out	Bypasses one gate delay to the clock path

Jumper No.	Solder Bridge	SC Default	DC Default	Dual Settings	Description
JP30	✓	Out	Out	Out	Used to insert additional gate delays to the clock path
JP31	✓	In	In	In	Bypasses two additional gate delays to the clock path (WRT_CLK2)
JP32	✓	Right	Right	Right	Allows the REN (read enable) on the FIFO to be controlled by the FF and EF (FIFO full and FIFO empty) signals, or to be connected directly to ground, which is the default setting
JP33	✓	Up	Up	Down	Allows the read CLK on FIFO2 to be controlled via RCLKA (the read CLK for FIFO1) or a second read CLK generated by the PC (default)
JP34–JP41		In	In	In	For use with the ADC Analyzer software. Inserting these jumpers connects the upper eight MSBs to the lower eight MSBs, allowing multiplexing of both onto the data bus for acquisition by the PC.
JP42	✓	Out	Out	Out	Used if a single clock is passed from the ADC evaluation board to the FIFO for both channels of data

Table 6. Jumper Configuration

SCHEMATICES AND PCB MASK DATA

FIFO CONNECTOR

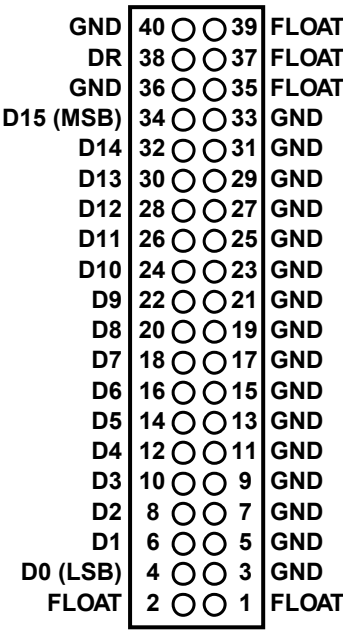


Figure 26. Single-Channel Connector Pin Diagram—Top View (HSC-ADC-EVAL-SC)

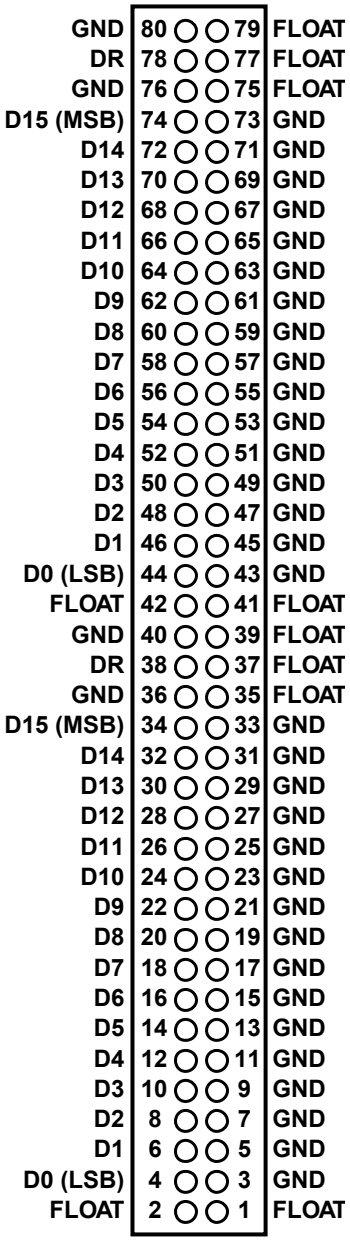


Figure 27. Dual-Channel Connector Pin Diagram—Top View (HSC-ADC-EVAL-DC)

PCB SCHEMATIC

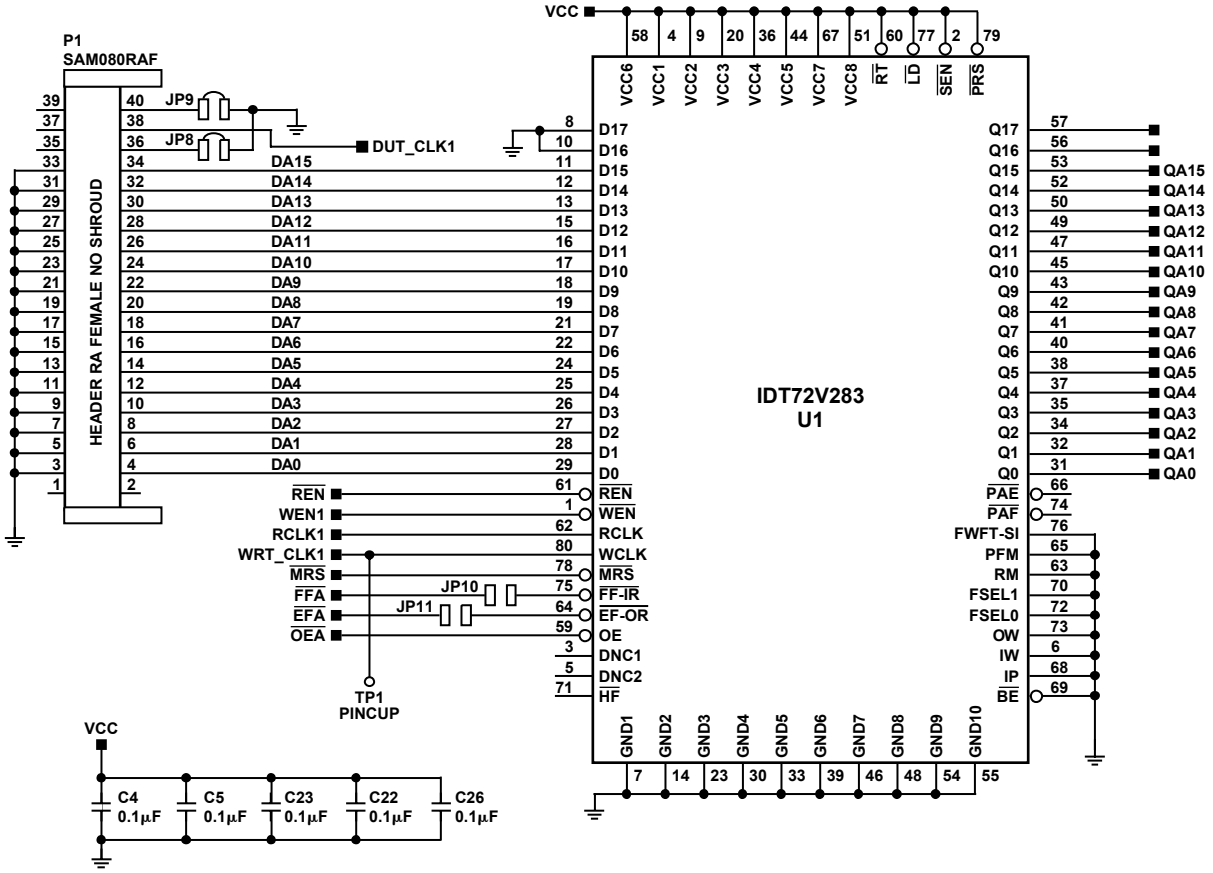


Figure 28. PCB Schematic

PCB SCHEMATIC (CONTINUED)

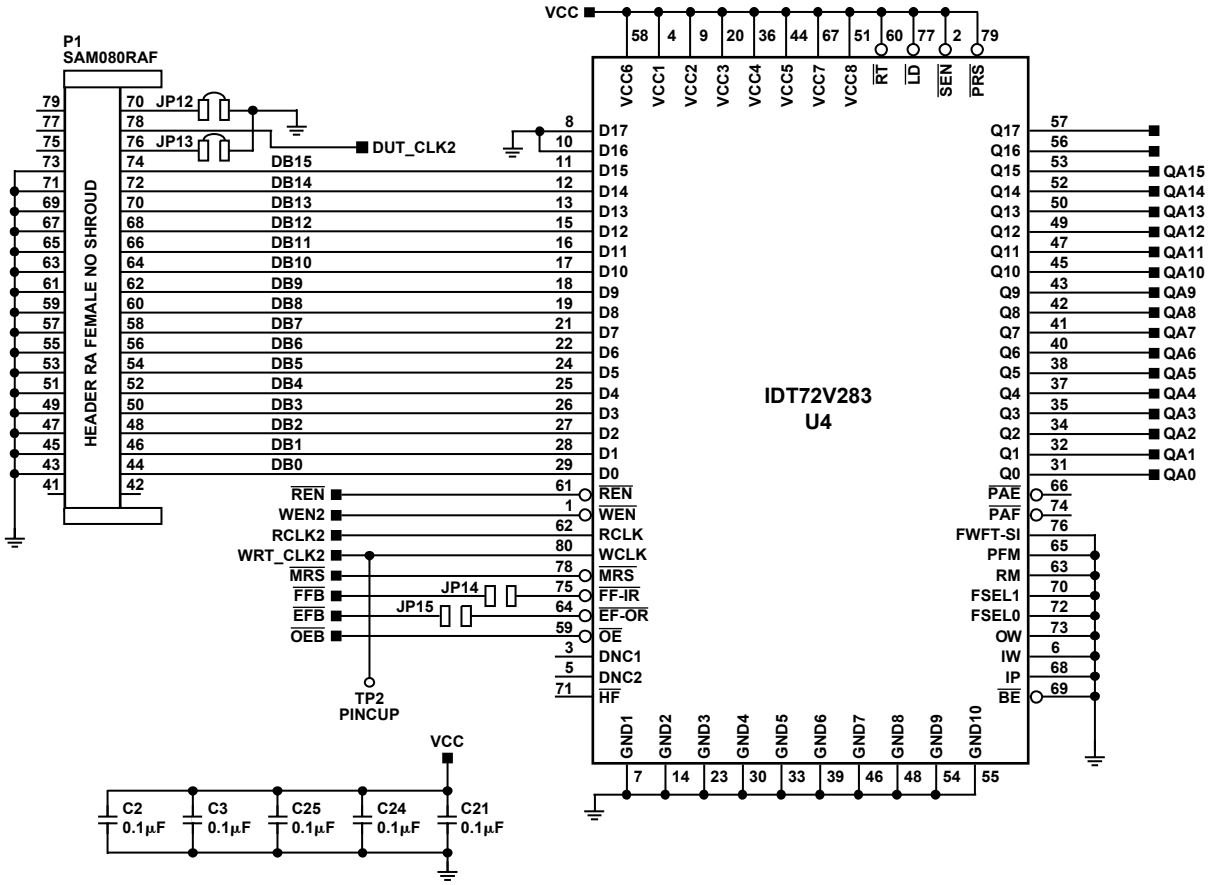


Figure 29. PCB Schematic (Continued)

PCB SCHEMATIC (CONTINUED)

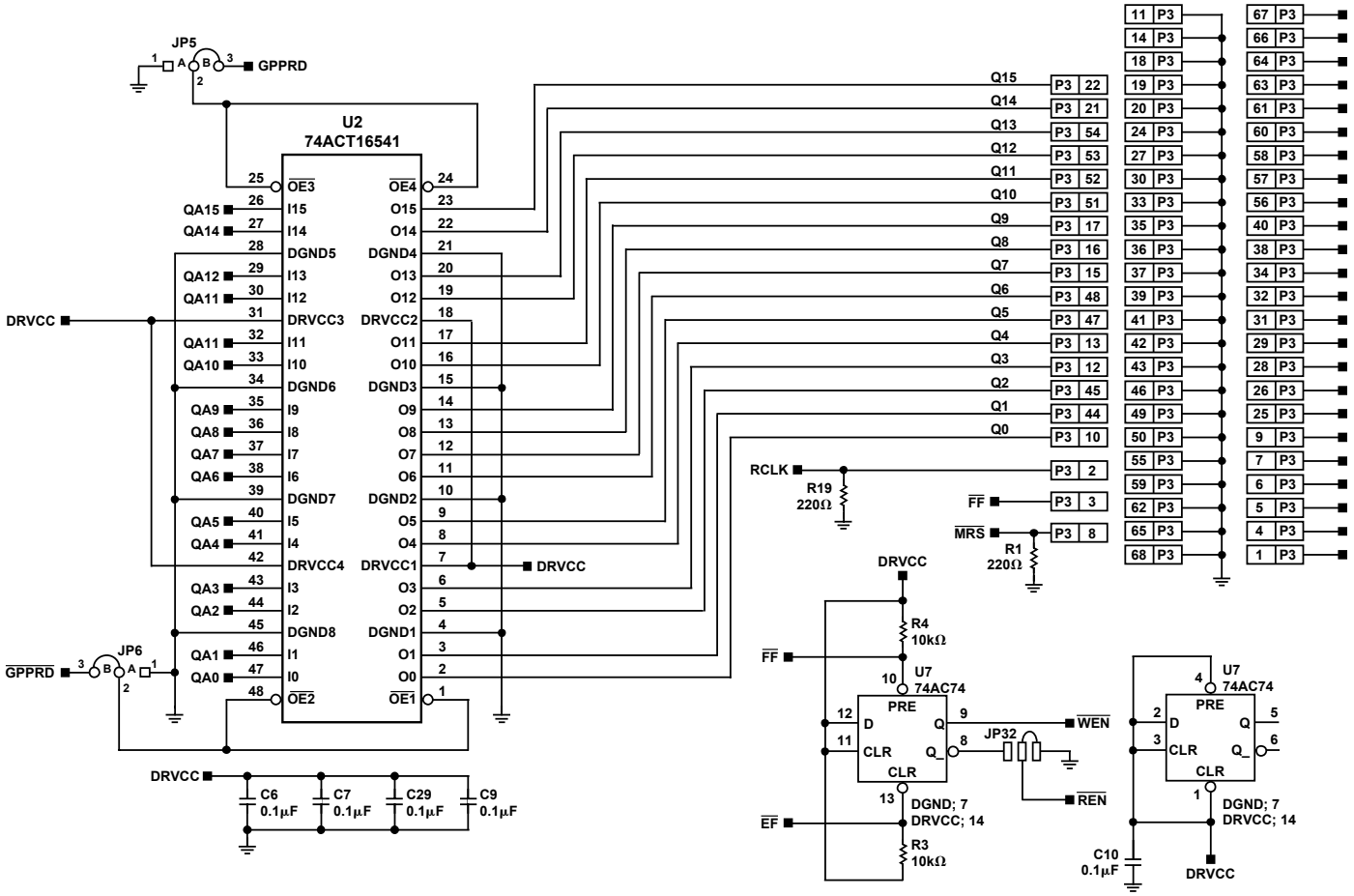


Figure 30. PCB Schematic (Continued)

PCB SCHEMATIC (CONTINUED)

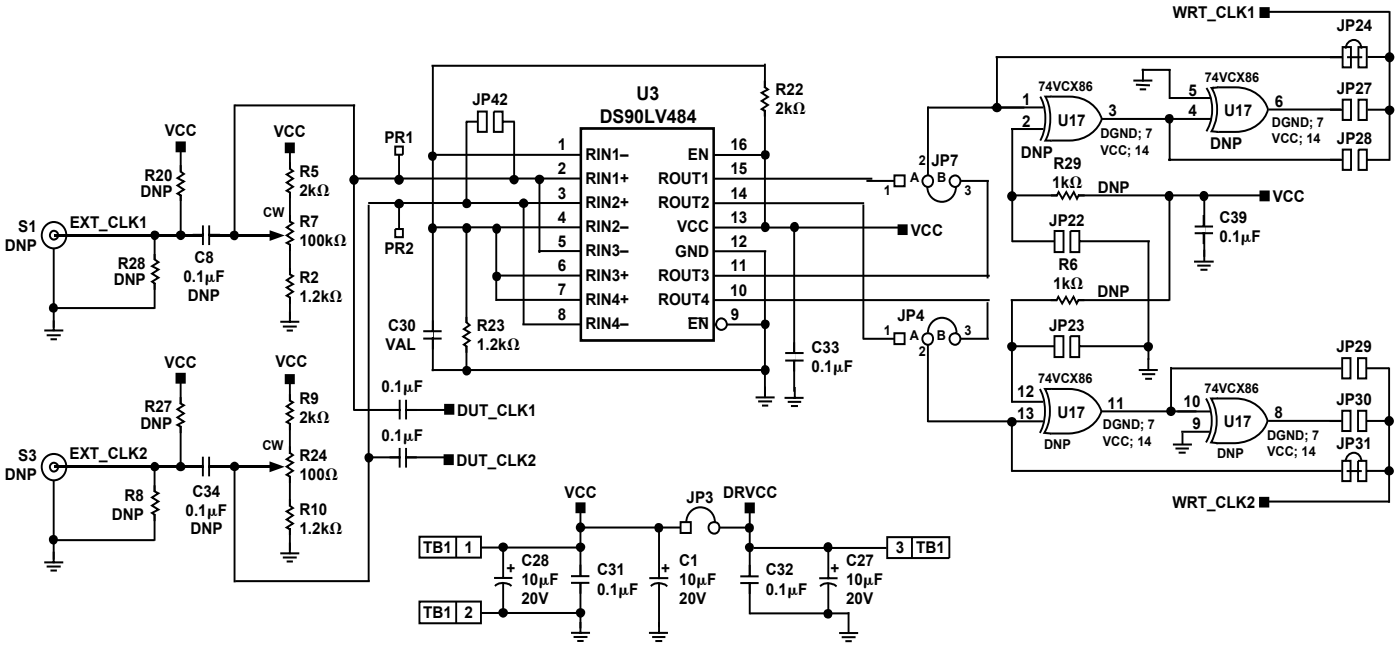


Figure 31. PCB Schematic (Continued)

PCB SCHEMATIC (CONTINUED)

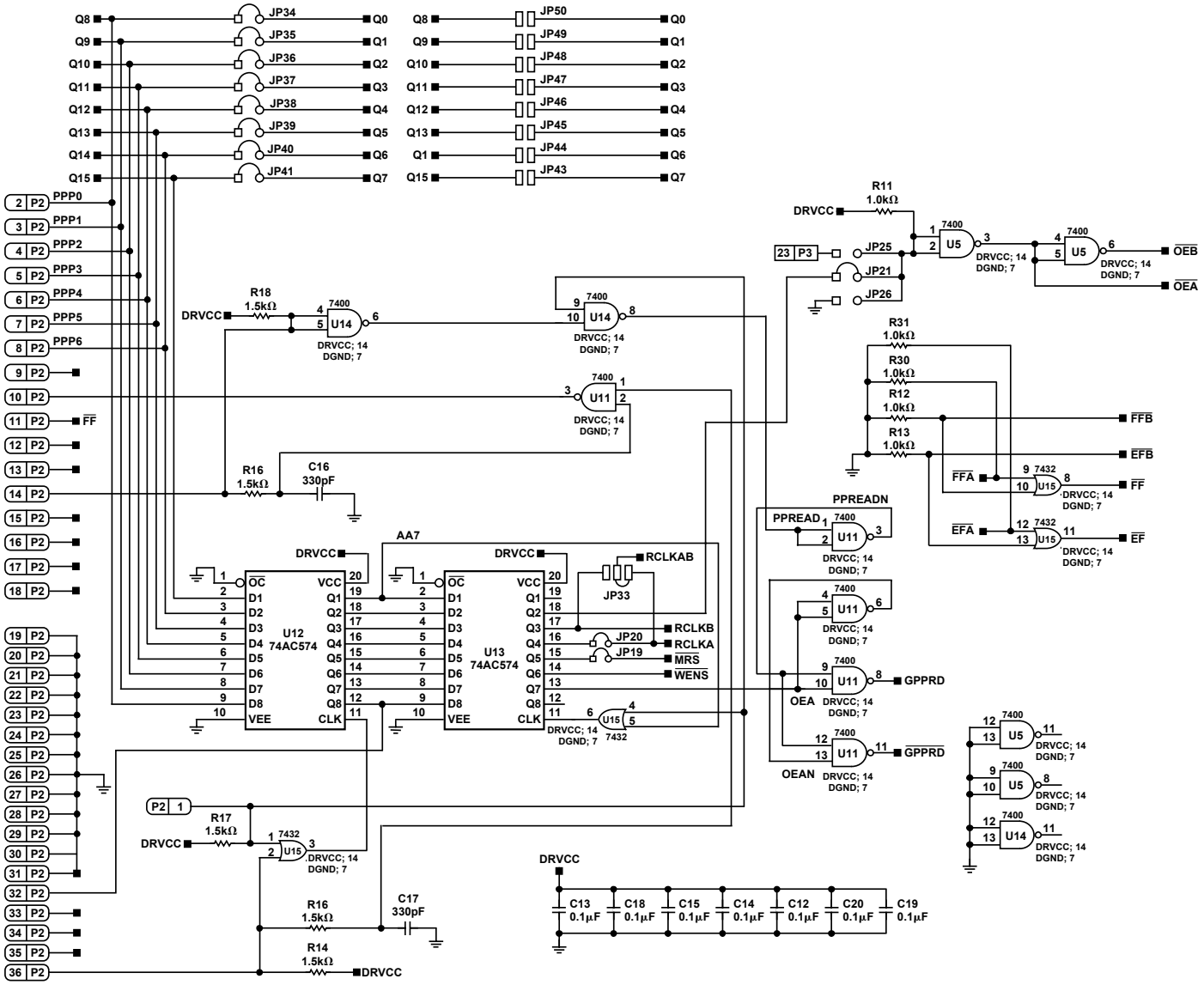


Figure 32. PCB Schematic (Continued)

PCB SCHEMATIC (CONTINUED)

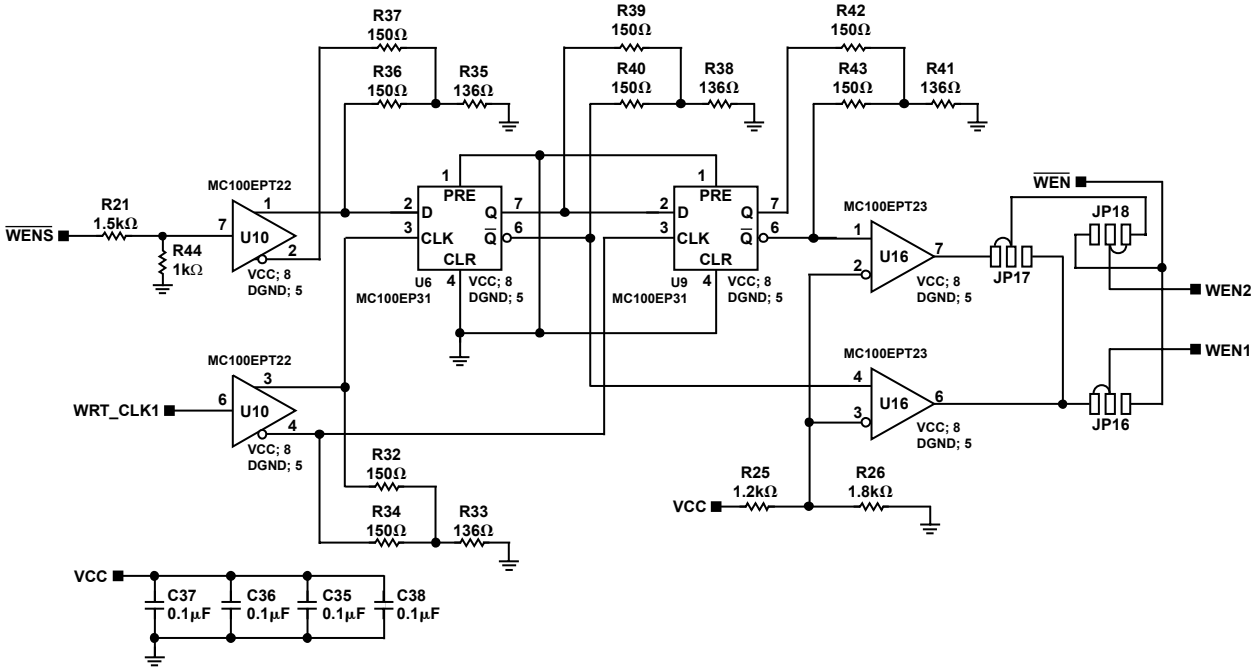


Figure 33. PCB Schematic (Continued)

ASSEMBLY—PRIMARY SIDE

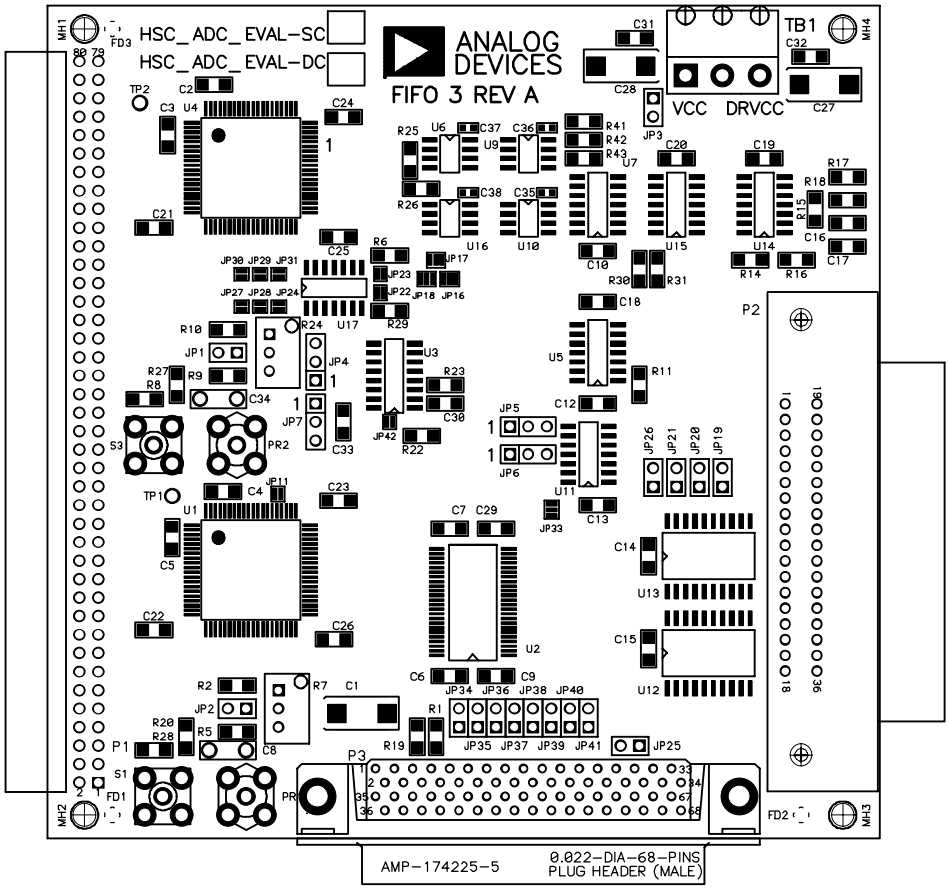


Figure 34. Assembly—Primary Side

ASSEMBLY—SECONDARY SIDE

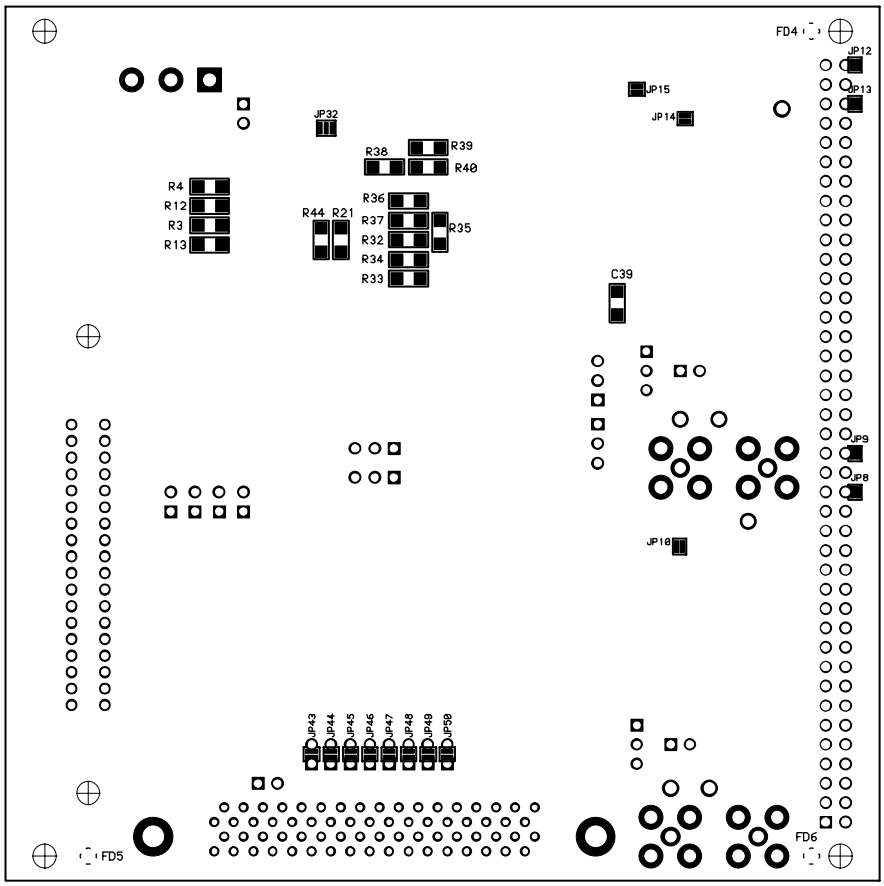


Figure 35. Assembly—Secondary Side

FABRICATION FIFO 3

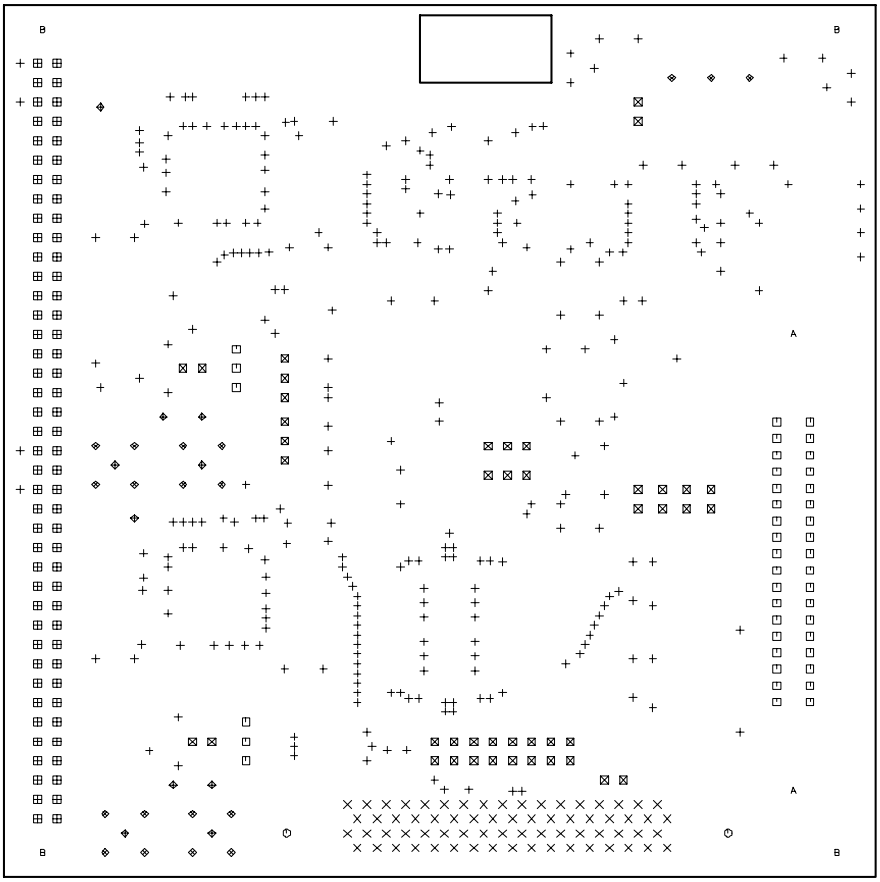


Figure 36. Fabrication FIFO 3

SILKSCREEN—PRIMARY SIDE

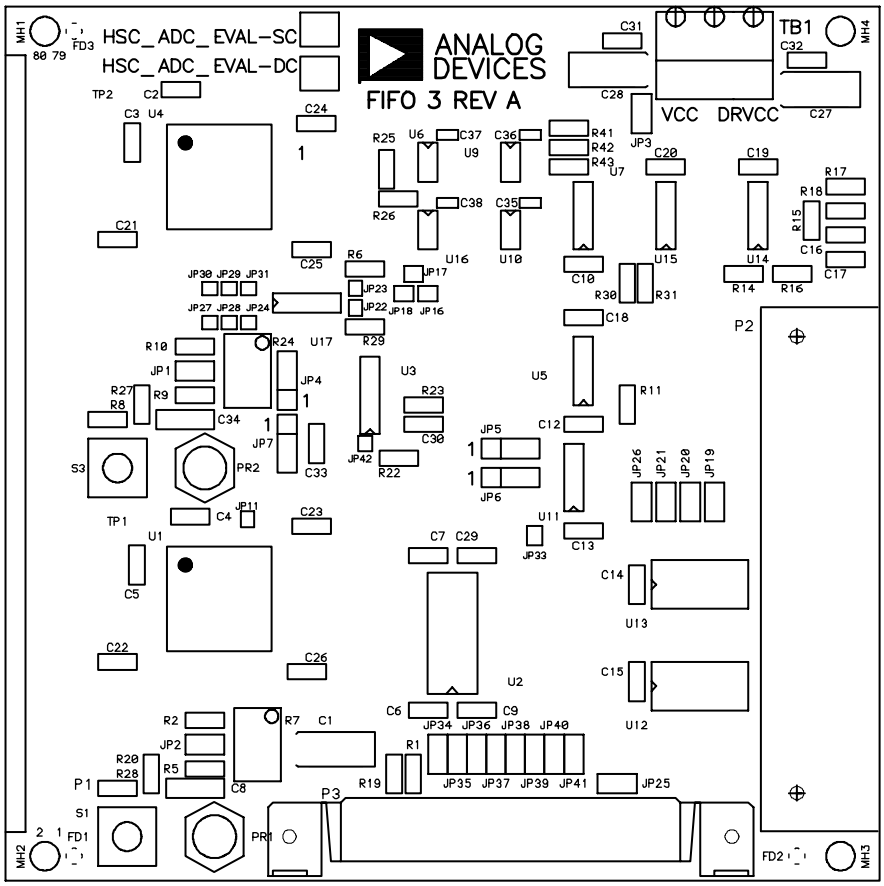


Figure 37. Silkscreen—Primary Side

SOLDERMASK—PRIMARY SIDE

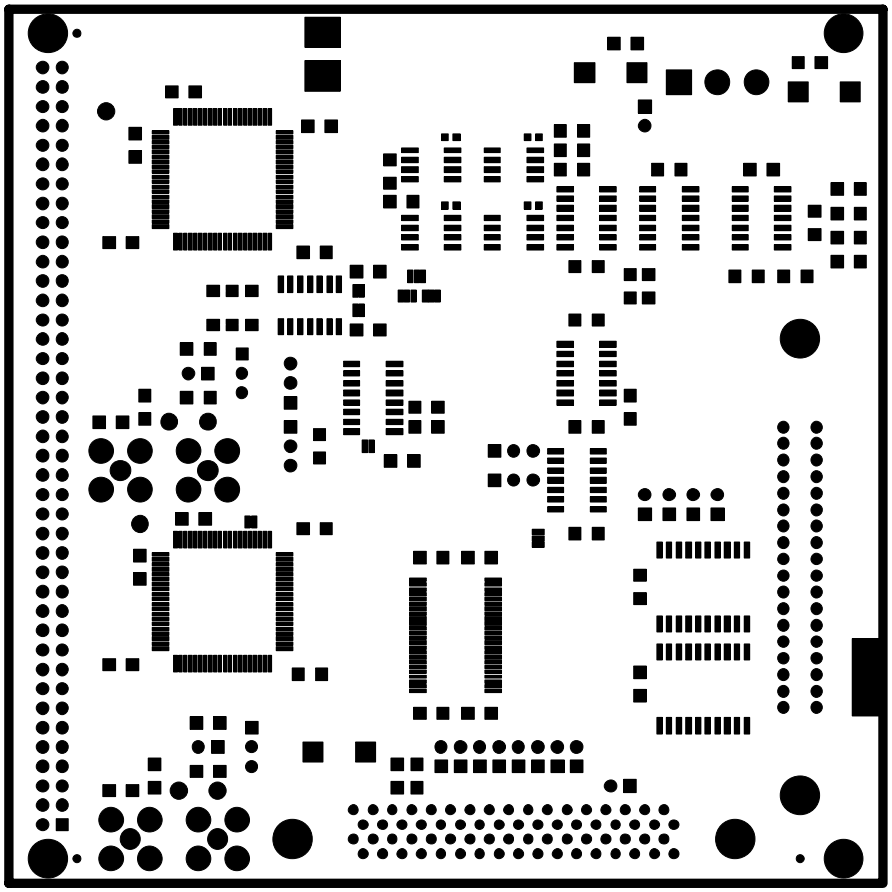


Figure 38. Soldermask—Primary Side

LAYER 1— PRIMARY SIDE

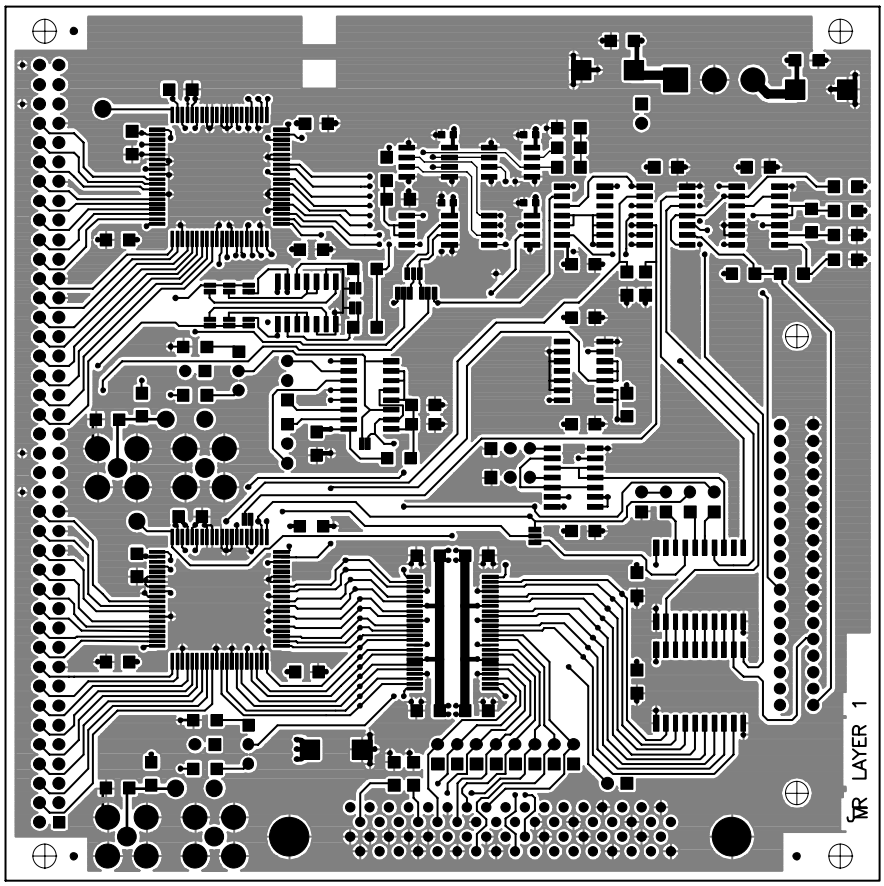


Figure 39. Layer 1—Primary Side

LAYER 2—GROUND PLANE

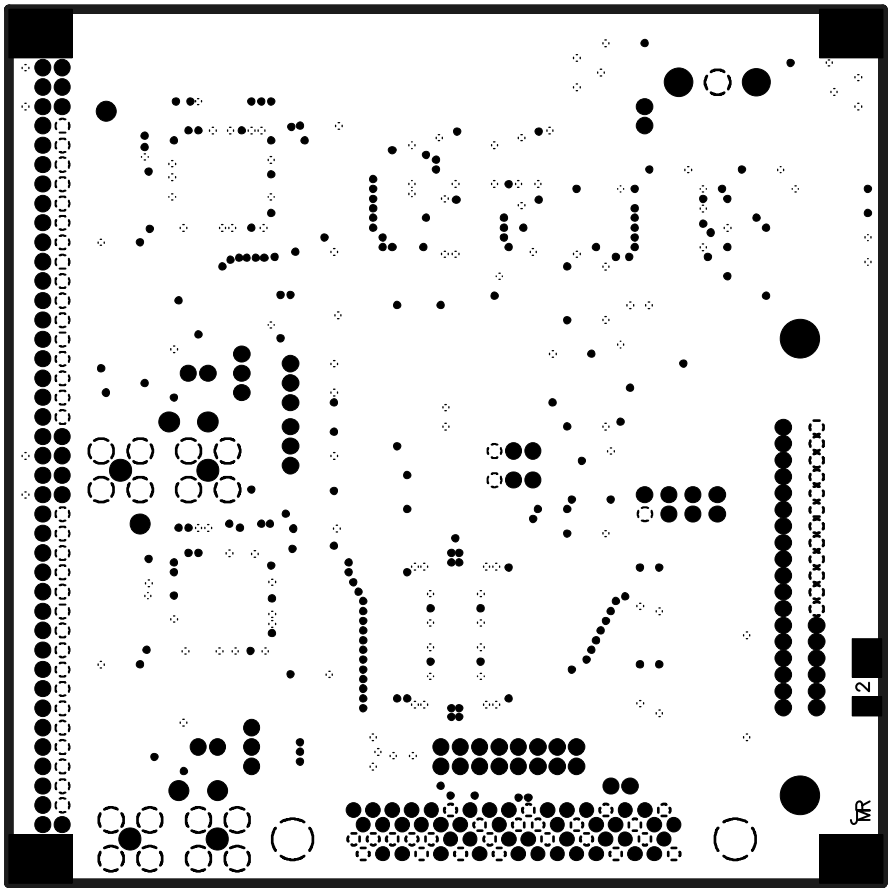


Figure 40. Layer 2—Ground Plane

LAYER 3—POWER PLANE

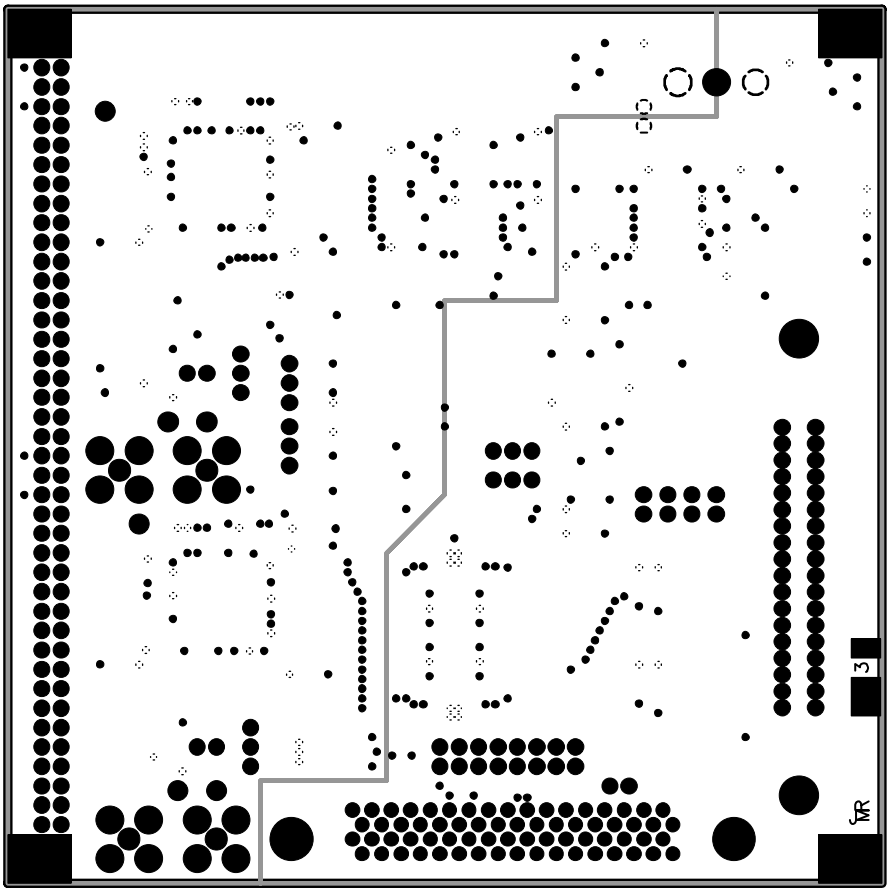


Figure 41. Layer 3—Power Plane

LAYER 4—SECONDARY SIDE

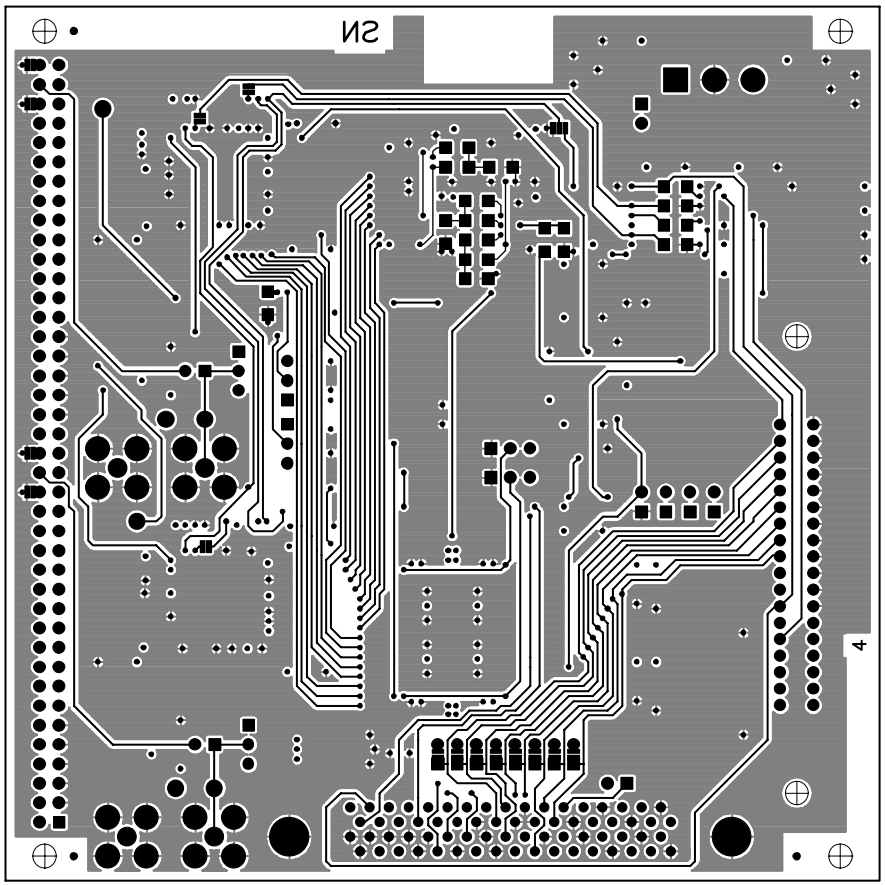


Figure 42. Layer 4—Secondary Side

SOLDERMASK— SECONDARY SIDE

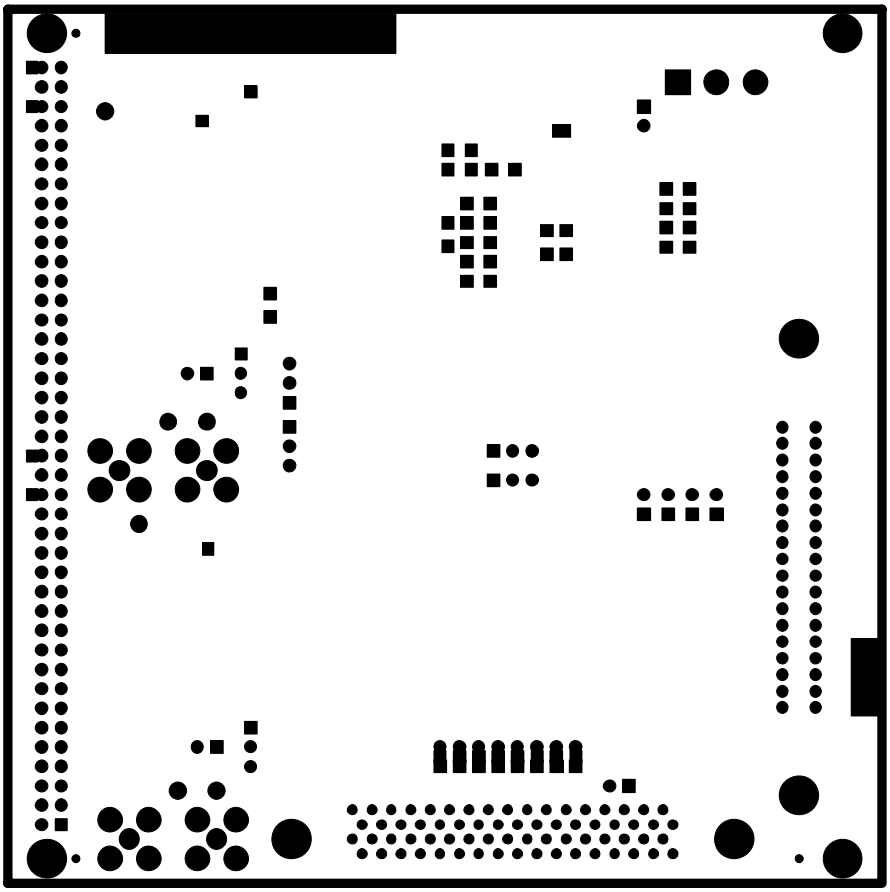


Figure 43. Soldermask—Secondary Side

SOLDER PASTE—PRIMARY SIDE

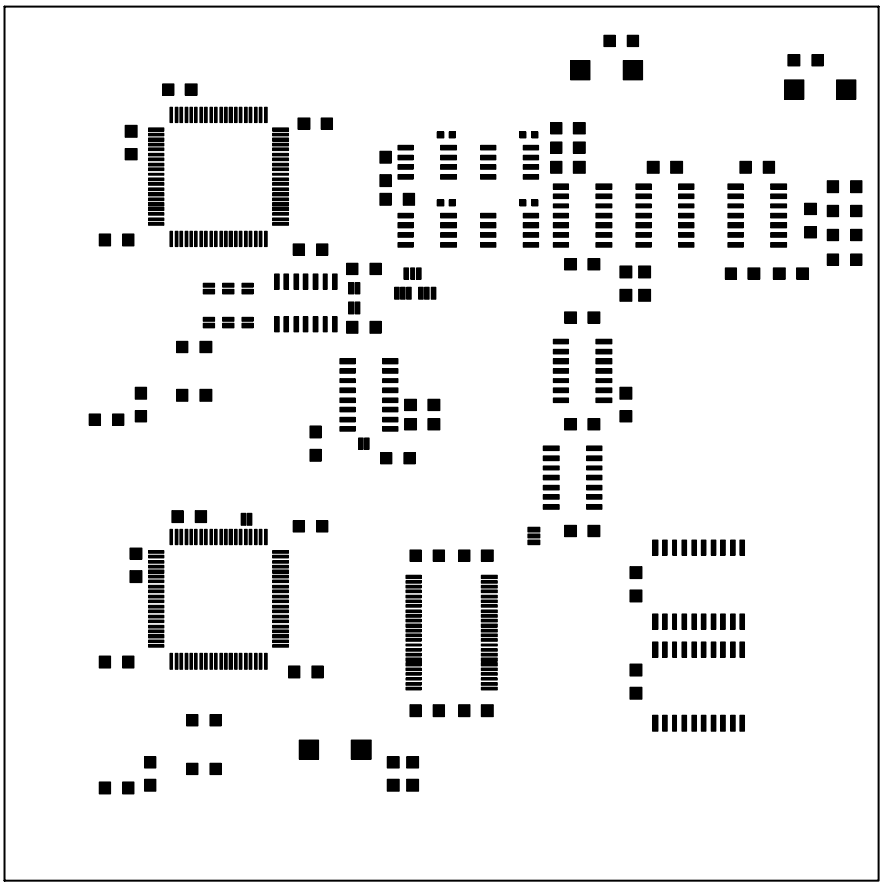


Figure 44. Solder Paste—Primary Side

SILKSCREEN—SECONDARY SIDE

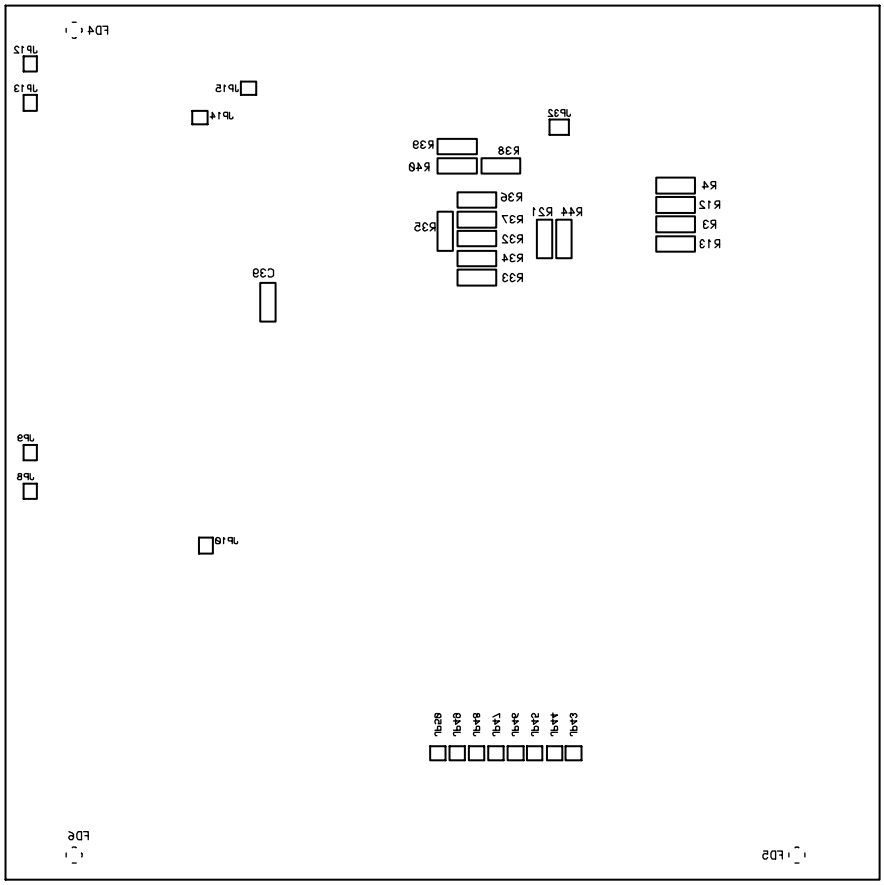


Figure 45. Silkscreen—Secondary Side

SOLDER PASTE—SECONDARY SIDE

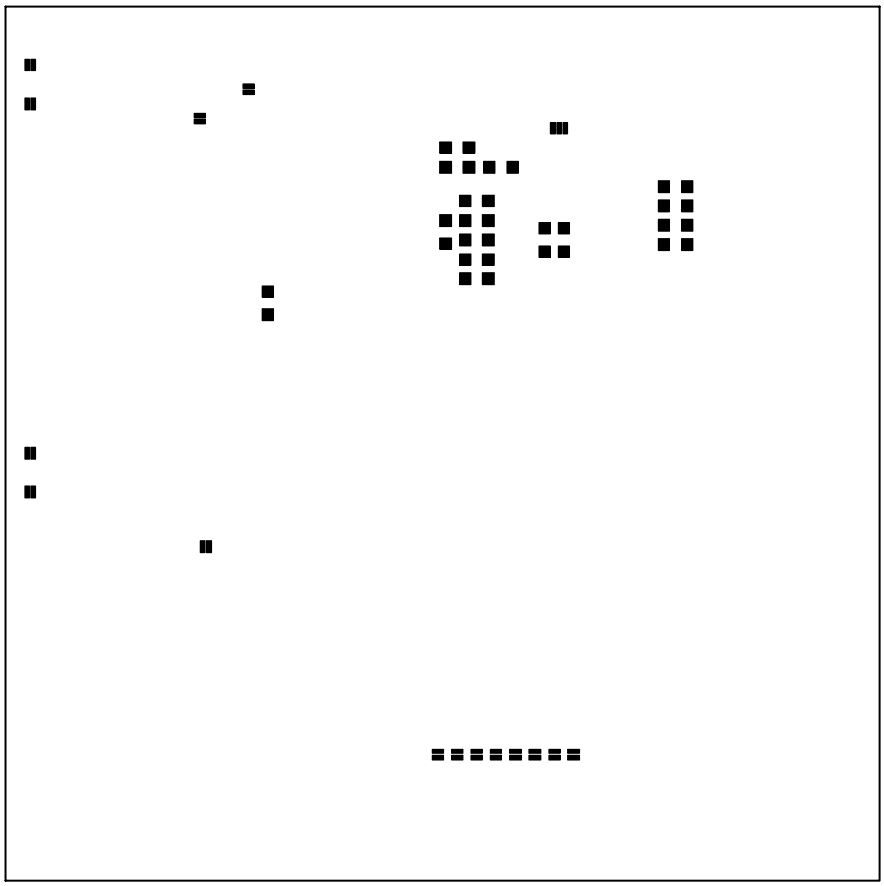


Figure 46. Solder Paste—Secondary Side

ASSEMBLY—PRIMARY SIDE

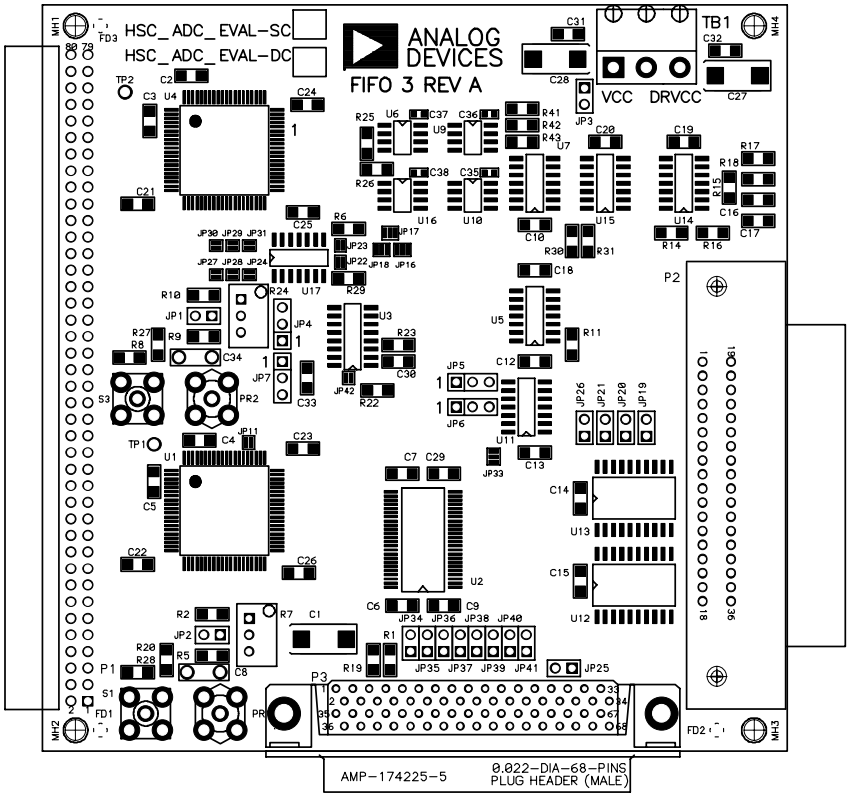


Figure 47. Assembly—Primary Side

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Ordering Guide

Model	Temperature Range	Description
HSC-ADC-EVAL-SC	25°C (Ambient)	Single FIFO Version of Evaluation Kit
HSC-ADC-EVAL-DC	25°C (Ambient)	Dual FIFO Version of Evaluation Kit
AD922XFFA	25°C (Ambient)	Adapter for AD922x Family (Included in Evaluation Kit)
AD664XFFA	25°C (Ambient)	Adapter for AD664x Family (Included in Evaluation Kit)
AD9432FFA[1]	25°C (Ambient)	Adapter for the AD9432 (Not included in Evaluation Kit)
AD9283FFA[1]	25°C (Ambient)	Adapter for the AD9283 and AD9057 (Not included in Evauation Kit)
AD9071FFA[1]	25°C (Ambient)	Adapter for the AD9071 (Not Included in Evaluation Kit)
AD9059FFA[1]	25°C (Ambient)	Adapter for the AD9059 (Not Included in Evaluation Kit)
AD9051FFA[1]	25°C (Ambient)	Adapter for the AD9051 (Not Included in Evaluation Kit)
LG-0204A[1]	25°C (Ambient)	Adapter for the AD10xxx and AD13xxx Families (Not Included in Evaluation Kit)

[1] If an adapter is needed, send an email to highspeed.converters@analog.com with the part number of the adapter and a mailing address.

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